

Best Practices for Thermal Modeling in Microelectronics with Natural Convection Cooling: Sensitivity Analysis

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Abstract

A detailed sensitivity study was carried out on various key parameters from a high precision numerical model of a microelectronic package cooled by natural convection, to provide rules for the thermal modeling of microelectronic packages subjected to natural convection heat transfer. An accurate estimate of the junction temperature, with an error of less than 1°C, was obtained compared to the experimental data for the vertical and horizontal orientations of the test vehicle in the JEDEC Still Air configuration. The sensitivity study showed that to have an accurate estimate of the temperature, the following elements should be present in the thermal model: radiation heat transfer in natural convection cooling; a computational fluid dynamics analysis to find realistic convection coefficients; detailed models of the high conductivity elements in the direction of the heat flow towards the environment; and finally precise values for the thicknesses of layers and the thermal properties of the substrate and the printed circuit board.

Keywords

Computational Fluid Dynamics, Computational Heat Transfer, Microelectronic Packaging, Natural Convection, Radiation, Thermal Analysis, Thermal Management

1. Introduction

The performance of microelectronic systems deteriorates rapidly when their temperature exceeds a certain limit. For some JEDEC standards used in qualification and reliability tests, operating temperature limits are set, for example, to

125°C for processors and 85°C for memory chips. The purpose of thermal management is to maintain throughout the equipment a temperature distribution with limited variations above the recommended limits. The advancement in IC package development driven by the increase of transistor density and miniaturization makes the task of the packaging designer more challenging.

The key to successful thermal management is the ability to obtain complete and accurate temperature data under realistic operating conditions. Collecting temperature data by direct measurements (e.g. thermocouples) is the most commonly used method, but it is limited by the number of measurement points and the small size of the components. Infrared Thermal Imaging (IR) alleviates some of these problems by providing complete external temperature mappings. However, this approach can be time-consuming and can only be applied after the design is complete and the parts have been fabricated. It is therefore important to have thermal models and numerical simulation tools that can provide the temperature profile of the chips to achieve high-quality designs before prototyping or manufacturing.

Several studies have been conducted to thermally model microelectronic packages [1]. Analytical methods can be used in simple cases such as isothermal or adiabatic flat plates in horizontal or vertical orientations, but these analytical methods have obvious limitations for complex geometries or thermal boundary conditions [2]. Numerical methods are frequently used for thermal simulations of electronic packages [3]. Most of these numerical methods use the finite element method [4], the finite volume method [5], or the finite difference method [6]. Many of these studies address only the conduction in the solid and assume or estimate the convection by empirical methods [7] [8], which are generally obtained by only considering the average temperature difference between the surfaces and the ambient environment. The variations of the cooling airflow velocity due to geometric changes are often neglected because it is difficult to take them into consideration. In addition, the radiation is most of the time neglected for low power applications [9], although there is little published information about the level of power, or about the temperature difference between surface and ambient environment, such the radiation has to be taken into account.

The objective of this study was to perform a sensitivity analysis on our coupled (conjugate) methodology between a highly accurate conduction model and a computational fluid dynamics (CFD) model, which was reported in [10] [11] to be highly accurate when compared to temperature measurements on actual hardware. The sensitivity analysis was performed using a one-factor-at-a-time approach to evaluate the influence of model features or parameter values on the accuracy of the simulation results. Our aim is to identify the key factors to consider for accurate thermal modeling in microelectronics packages with natural convection cooling.

We present in this paper a method that enables an accurate prediction of the temperature field in a microelectronic package mounted on a printed circuit board (PCB) when it is cooled by natural convection to a thermal steady state.

This configuration allows the estimate of the standard junction-to-ambient (θ_{JA}) thermal resistance in natural convection, which is useful to evaluate the relative thermal performance of microelectronic packages [12]. Our method is based on the coupling of a conduction model and of a fluid flow model. It performs well because of the high level of geometrical details in the conduction model, and because of the high resolution of the airflow and heat transfer models around the package. The accuracy of the conduction model within the solid domain is improved by a fine spatial discretization, while the precision of the convection model in the fluid domain results from a good spatial discretization of the thermal boundary layer. Using this high precision model, we evaluate the impact of the variation of several parameters on the temperature field in the package assembly, in comparison to experimental measurements. These parameters include the lid conductivity; the thermal interface material (TIM) thickness and conductivity; the underfill conductivity and the constriction resistance in the calculation of the equivalent resistance of the underfill layer with the interconnects (flux tube model); the laminated substrate copper distribution and thickness variability; the substrate core and dielectric conductivity; the presence of vias in the substrate dielectric and in the substrate core; the ball grid array (BGA) conductivity; the PCB thickness variability and emissivity; the PCB dielectric material in-plane and out-of-plane conductivity; the presence of thermal vias in the PCB; the use of empirical formulas for convection modelling; the consideration of radiation heat exchange and the still air chamber inclination. This study highlights the most important features to take into account for the construction of precise thermal models.

The paper is divided into eight sections. A review of the literature on the sensitivity studies around thermal issues in microelectronics packaging is presented in Section 2. Section 3 describes the detailed methodology of the two-way coupling between the conduction model and the fluid flow model. The acquisition of experimental data for the validation of the methodology is presented in Section 4. The results from the detailed numerical models are discussed in Section 5. Section 6 presents the validation of the numerical models, by comparing the results of the simulations from Section 4 with the experimental data from Section 5. The sensitivity analysis is discussed in Section 7 (key parameters) and in Section 8 (results and discussion).

2. Related Work

Sensitivity studies have been carried out by some authors for thermal issues in microelectronic packaging, but the list of parameters studied is not as exhaustive as what is targeted in the present study. Reference [13] presents an efficient lid design for a 3D stacked flip-chip package that increases the contact surface of the TIM between the top chip and the lid for a better heat conduction transfer. A sensitivity analysis is presented for the thermal resistance of five key structures (TIM, underfill/C4 composite between the two chips and the lower chip to sub-

strate, substrate and seal band), to identify the most critical structure for the thermal performance of the package. This study concluded that the chip-to-chip thermal resistance in the 3D package was most critical and could be reduced by improving the thermal conductivity of the underfill material, increasing the C4 density and by decreasing their height. Therefore, an accurate assessment of the chip-to-chip thermal resistance and of the TIM thermal resistance is required for accurate temperature predictions in similar 3D packages. However, in this study only the conduction was treated with a compact model, which has the advantage of producing a fast approximate solution with very few details but leaves out many important details, such as the effect of radiation, for instance. The validation of the model was performed by comparing the experimental thermal resistivity value from sensors at different positions in the chip (center, near edge and edge) and the data from numerical model. However, the numerical model was solved by setting a uniform convection coefficient on the top of the lid ($1000 \text{ W/m}^2\text{K}$) and the bottom of the substrate ($10 \text{ W/m}^2\text{K}$), neglecting edge effects and fluid velocity fluctuations on surfaces.

The heat dissipation of a microelectronic device mounted on a four-layer PCB cooled by natural convection was studied in references [14] and [8]. In the first study [14], a finite element conduction model was used, with empirical formulas for estimating the fluid heat transfer coefficients. In the second study [8], a CFD model was used to solve the conjugated solid/fluid heat transfer problem, with sensitivity analysis on the use of empirical model for the convective heat transfer, and on the PCB features (such as the number of copper layers, thermal vias and thermal BGA). These results showed that using a CFD methodology leads to better predictions compared to using empirical model to estimate fluid heat transfer coefficients, and that the PCB structures such as thermal vias, thermal BGAs and copper layers have a considerable influence on the equilibrium temperature field.

Reference [15] has presented a sensitivity analysis of conjugate heat transfer for cooling electronic devices for heat sink characterization and system-level thermal design optimization. The parameters of this study comprised: the distance between the top of the heat sink and the enclosure (the gap), the angle of the flow (0° to 60°), the conductivity of the heat sink (25 to 430 W/mK) and the fluid flow velocity. The goal of this study was to minimize the thermal resistance of a heat dissipating component. These results showed that the minimal thermal resistance of the heat sink (8.1 K/W) was obtained with a minimum gap and a forced convection flow angle of 30° at a power of 9 W . The authors also showed that the resistance could be further reduced using a heat sink material with higher thermal conductivity.

Reference [16] has studied the conjugate heat transfer of a computer cooled by liquid. The study showed the variation of the maximum temperature with variations in the space between the chip and the heat sink, as well as the operating power between 15 W and 40 W . Hence, the maximum temperature was de-

creased by 38% using water in the enclosure, relative to the air cooling. Increasing the space between chip and heat sink reduced the temperature. However, beyond 50 mm, this increase in space had an impact of less than 1% on the temperature variation.

Table 1 summarizes the impact of the package thermal resistance (junction to cooling fluid) by varying by +10% the nominal value of continuous parameters and by taking into account or not in the simulations the discrete parameters, for the references cited above.

These studies show that some parameters (such as the number of copper layers, and the presence of thermal vias) have a much larger impact on the estimated thermal resistance than other parameters. While leaving important details out of the simulations can reduce accuracy considerably, adding unnecessary details consume more computing resources, sometimes with minimal benefits on accuracy. Therefore, there is a need for identifying key features for the construction of precise thermal models, which is the main goal of our study.

Table 1. Summary of the impact of the variation of some parameters in the literature.

Parameters	Nominal value	Relative variation of thermal resistance	References
PCB copper layers	2 vs. 4 layers	54%	[8] [14]
PCB thermal vias	On-off	14%	[8] [14]
Flow velocity	2 m/s	9.4%	[15]
Underfill/C4 (between the two chips) thermal resistivity	50 mm ² K/W	9.1%	[13]
Operating power	40 W	7%	[16]
TIM thermal resistivity	10 mm ² K/W	5.3%	[13]
Flow angle	0°	5%	[15]
CFD	On-off (empirical formulas)	2%	[8] [14]
Enclosure width	60 mm	2%	[16]
Distance between the heat sink and the enclosure	5.5 mm	1.1%	[15]
PCB thermal BGA	On-off	1%	[8] [14]
Substrate thermal resistivity	60 mm ² K/W	0.7%	[13]
Heatsink conductivity	151 W/mK	0.34%	[15]
Underfill/C4 (between the lower chip to substrate) thermal resistivity	75 mm ² K/W	negligible	[13]
Sealband thermal resistivity	600 mm ² K/W	negligible	[13]

3. Methodology

Our study uses the finite element method (FEM) for the heat conduction inside the package and the finite volume method (FVM) for the air convection in the volume surrounding the package. The FEM enables more precise solutions by increasing the order of the elements and by refining the mesh locally, while the FVM is robust for solving the non-linear conservation laws which appear in fluid transport problems.

The full heat transfer problem was simulated using a two-way (conjugate) coupling methodology between a FEM conduction model and an FVM fluid model. The detailed numerical models are presented in Section 5. The interaction between the two models was implemented through exchanges of temperature fields and convection coefficients at the boundaries between the solid domain and the fluid domain.

The two-way coupling methodology involved iterating through the following steps: first, the heat transfer in the conduction model was solved with Ansys APDL [17] by applying uniformly an initial estimate of the heat transfer coefficients (obtained for instance from empirical formula [18]) at each solid-fluid interface. Second, the temperature field at the solid-fluid interfaces calculated in the conduction model was applied as a boundary condition in the FVM simulation (see Equation (2)), which was solved with Ansys Fluent [19] to determine the velocity and pressure fields around the package. For each solid-fluid interface FVM element, the total heat transfer coefficient h_{tot} was calculated using

$$h_{\text{tot}} = \frac{q_{\text{wall}}}{T_{\text{element}} - T_{\text{ambient}}} \quad (1)$$

where q_{wall} is the total heat flux including convection and radiation, T_{element} is the temperature of each element at the solid-fluid interface and T_{ambient} is the fluid temperature at infinity. The heat transfer coefficients were transferred to the FEM model (see below). Third, the heat transfer coefficients were applied to all elements in the conduction model, which was solved again. Several iterations of the second and third steps were executed, until the calculation was terminated after the third step when the difference of the maximum temperature between two successive iterations was less than 0.2 K. **Figure 1** shows typical convergence data for two orientations of a package (horizontal and vertical).

The FEM and FVM meshes were non-conformal. We found that an effective way of transferring the temperature field from FEM to FVM was to fit the temperature distribution on each surface with a Gaussian function. The fitting equation of the FEM temperature field for each surface was

$$T(x, y) = A_i e^{-\left(\frac{(x-x_{0i})^2}{2\sigma_{xi}^2} + \frac{(y-y_{0i})^2}{2\sigma_{yi}^2}\right)} + B_i \quad (2)$$

where A_i , B_i , x_{0i} , y_{0i} and σ_{xi} and σ_{yi} are the fit constants for each surface i (the top of the lid and the top and the bottom of the PCB).

The FVM convection coefficients were transferred to the FEM by projecting

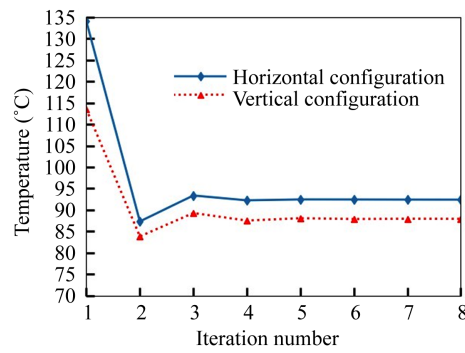


Figure 1. Convergence of maximum temperature versus iteration number, for 10 W power consumption, for two configurations: horizontal (solid line) and vertical (dotted line).

the convection coefficients from the FVM mesh to the FEM mesh at the solid-fluid interfaces using linear interpolation, by using a Delaunay triangulation of the FVM data, and performing linear barycentric interpolation at each FEM nodes.

4. Temperature Measurements

The validation of our calculation methodology was performed using experimental data obtained under the Integrated Circuits Thermal Test Method Environmental Conditions-Natural Convection (Still Air) (JEDEC JESD51-2) [12] standard test in natural convection heat transfer in a still-air ambient environment. The still air chamber had a volume of 0.028 m³. The 6.35 mm thick plastic walls were fabricated from transparent acrylic with low thermal conductivity and high emissivity. The chamber included a fixed thermocouple probe for measuring the internal air temperature. The standard JESD51-2 recommends an increase of the box volume if during the tests the temperature in the chamber increases by 10% or if the power exceeds 3 W, which was the case in our tests. This recommendation is justified by the fact that there could be convection on the exterior surfaces of the box impacting the thermal characterization. To verify this, type-T thermocouples were bonded internally to the corners of the box and at the center of each wall of the box to measure an eventual heat flux outside the box for heating powers above 3 W. Based on these results, it was decided to increase the domain of the CFD model to take into account the air volume outside of the box.

The test vehicle consisted of a test module mounted on a JEDEC standard PCB of dimensions 127 × 139.7 mm² by an array of BGA solder balls. The test module was composed of a silicon chip of dimensions 12.57 × 12.57 mm², flip-chip mounted on an organic substrate of size 55 × 55 mm². The interconnections between the chip and the substrate were a matrix of solder bumps (C4) filled with an underfill polymeric material to increase the mechanical integrity of the solder bumps. The module was stiffened by a 1 mm-thick copper lid that also served as a first-level heat sink. The lid was thermally coupled to the chip by a thin thermal interface material (TIM, approximately 15 μm thick) and attached

to the substrate with a silicone adhesive (seal band). There was an excess of the TIM during the attachment process that filled the gap between the lid and the underfill (Figure 2).

The silicon chip had nine heating elements and six *in-situ* resistance temperature detectors (RTD). These RTD were located at different positions on the chip: one at each corner and two at the center of the chip (Table 2). To better capture convection on external surfaces and thus validate our numerical model, eighteen type-T thermocouples were bonded to some exterior surfaces (top and bottom of the PCB and top of the lid). Their positions are listed in Table 2.

5. Numerical Models

In this paper, numerical simulations were performed using a specialized cloud software infrastructure (PACK [20]). Pack is high performance numerical simulation software used as an interface to other commercial numerical simulation software (such as Ansys APDL and Ansys Fluent). PACK allows the efficient

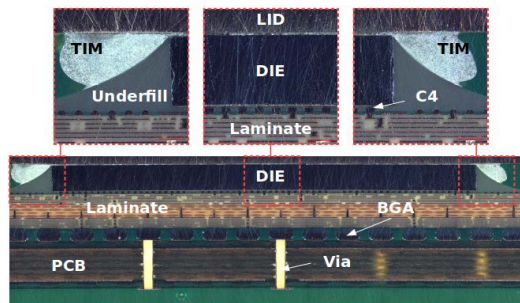


Figure 2. Optical micrograph of a cross section of the vehicle test, showing lid, die, substrate, BGA and PCB with a focus on C4, underfill and TIM bond line.

Table 2. Thermocouples locations.

		x (mm)	y (mm)	x (mm)	y (mm)
Top of the package	Lid center	0	0		
	Chip corner (over the lid)	-6	6	6	-6
	Lid corner	-20	20	20	-20
	PCB	-32	30	30	-32
<i>In-situ</i>	PCB corner	-56	51	51	-56
	Die Center	-1	0	1	1
	Die Corner	-4.5	-4.5	4.5	4.5
Bottom of the package	Die Corner	-4.5	4.5	4.5	-4.5
	Li center (under the PCB)	0	0		
	Chip corner (under the PCB)	-6	6	6	-6
	Lid corner (under the PCB)	-20	20	20	-20
	PCB	-32	30	30	-32
	PCB corner	-56	51	51	-56

generation of parametric numerical models that use advanced pre- and post-processing capabilities using an object-oriented programming model.

5.1. FEM Model

The PACK infrastructure was used to build the conduction model with the Ansys APDL finite element software [17]. In this model, we chose to use the finite element method especially for the accuracy and complexity of the geometry of our test module (Figure 3). The conduction model represents the test module with the PCB, as explained in Section 3.

The properties of the materials were assigned individually to each element according to the position of the element in a given volume. The C4 and BGA were modeled with a homogenized layer with equivalent thermal properties. The equivalent out-of-plane resistance of these layers was the sum of two resistances in parallel, for the interconnection and the surrounding material. In-plane, it was assumed to equal the surrounding material thermal resistance (underfill for the C4 and air for the BGA). The thermal resistances of the C4 and BGA interconnections was calculated with the flux tube formula [21], given by

$$R_{\text{ball}} = \frac{(1-\varepsilon)^{1.5}}{2d_{\text{Ball}}} \cdot \left(\frac{1}{\lambda_1} + \frac{1}{\lambda_2} \right) + \frac{4h_{\text{Ball}}}{\lambda_{\text{Ball}}\pi d_{\text{Ball}}^2}, \quad (3)$$

with,

$$\varepsilon = \sqrt{\frac{\pi d_{\text{Ball}}^2 N}{4A}} \quad (4)$$

where λ_1 , λ_2 and λ_{Ball} are the thermal conductivities of the top layer, bottom layer, and the C4 or BGA, h_{Ball} is the C4 or BGA height, d_{Ball} is the C4 or BGA diameter, N is the number of C4 or BGA and A is the total area of the chip or substrate. Equation (3) is valid for $0 < \varepsilon \leq 0.3$. Table 3 summarizes the dimensions and thermal properties of the materials used in the different layers.

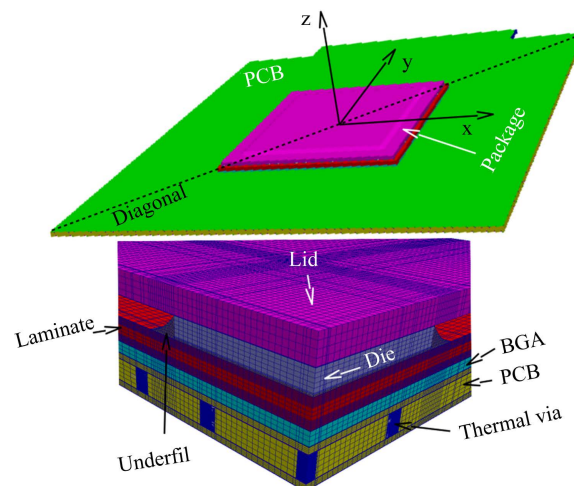


Figure 3. Description of the FEM Model with a focus on the specific mesh of 3,324,148 elements and 3,402,667 nodes.

Table 3. Material properties.

Materials		Dimensions	Conductivity (W/m K)	
			in-plane	out-of-plane
PCB	Prepeg	226 μm thick	0.8	0.25
	Core	927 μm thick		
	Copper	30 μm thick	385	
BGA Equivalent		400 μm diameter 1 mm pitch 500 μm thick	1×10^{-3}	6.64
C4 Equivalent		100 μm diameter 200 μm pitch	0.7	5.98
Substrate	Copper	15 μm thick	385	
	Core	400 μm thick	0.65	
	Diel.	33 μm thick	0.49	
Underfill		65 μm thick	0.65	
Die (Silicon)		785 μm thick	148	
TIM		15 μm thick	2.6	
Sealband		4 mm width	3.2	
Lid		1 mm thick	385	

One of the key elements in the realization of the high precision conduction model was the detailed modeling of the organic substrate. Substrate layer design files were used to model accurately the copper distribution and the vias of each layer in the organic substrate by superimposing the substrate design file and the mesh. In this approach, a rectangular background grid (pixels) was constructed based on black and white images of each layer of the organic substrate. The pixel count within each finite element is used to calculate the effective isotropic material properties based on the local concentration of copper and dielectric. This, effectively, forms a map of the material properties across each layer of the organic substrate [21]. The local thermal conductivity properties $\lambda_{eff,n}$ of each finite element in the substrate were calculated using

$$\lambda_{eff,n} = \beta_n \cdot \lambda_{\text{Copper}} + (1 - \beta_n) \cdot \lambda_{\text{Dielectric}} \quad (5)$$

where β_n is the area fraction of element n covered by copper, λ_{Copper} and $\lambda_{\text{Dielectric}}$ are the thermal conductivity of copper and dielectric material. This method allows for a more accurate representation of the organic substrate material distribution than the standard homogenization approach. Each layer of the PCB was modeled with homogeneous layers and the thermal vias were explicitly represented. The heat flux was applied uniformly at the bottom of the die as a source term. The simulations were performed in the steady state.

5.2. FVM Model

Ansys Fluent was used to build the FVM model [19]. The FVM model was composed of the air inside the chamber, the chamber itself, and the air outside the still air chamber (Figure 4). The dimensions of the outer domain of the still air chamber were taken large enough to put the temperature in the laboratory as boundary conditions (0.61 m away of each side of the still air chamber except the face that sits on the lab table, which had a gap of 25.4 mm).

A surface-to-surface radiation model [19] for the resolution of radiation heat transfer as well as the $k-\varepsilon$ turbulent model for the transport problem [19], were chosen. The resolution of the energy equation was done in our model in conjunction with the $k-\varepsilon$ turbulent model derived from the Navier-Stokes equations [19]. For more details on numerical models and hypotheses, see reference [10].

6. Comparison of Numerical Results and Experimental Data

The validation of our numerical model was done by comparing the results of the simulations with the experimental data (Figure 5). The comparison was performed on the diagonal line of three surfaces (the top of the lid, the die junction and the bottom of the PCB) and for two orientations (horizontal and vertical).

The results presented in Figure 5 show that our two-way coupled methodology provides accurate estimates of the temperature fields for both the vertical and the horizontal orientations of the test vehicle. For more details on the validation of our numerical model, see reference [11].

7. Sensitivity Study

In order to contribute to the definition of best practices in the modeling of packages cooled by natural convection, a sensitivity study was performed on key parameters of our numerical model in order to evaluate their impact on the accuracy of the simulation results. These parameters can be classified into two types: continuous parameters where the impact of a variation of +10% of their nominal value was evaluated (e.g. variations in thickness and thermal conductivity) and discrete parameters where the impact of their taking into account or not in the simulations was evaluated (e.g. the presence of vias and the use of copper distributions). See Table 4 for the full list.

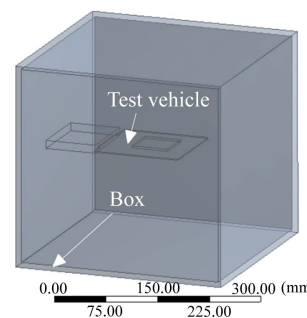


Figure 4. Description of the FVM model, excluding the volume outside of the chamber (box).

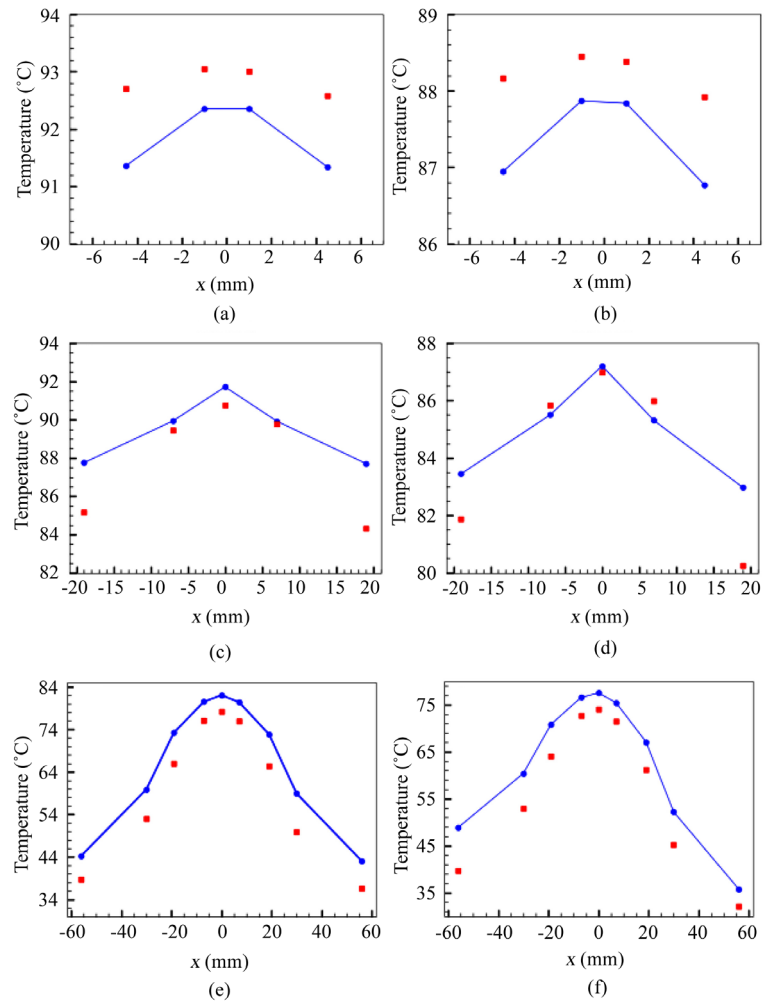


Figure 5. Comparison of the simulated temperature (round markers) and measurements (square markers) in the horizontal ((a), (c) and (e)) and vertical ((b), (d) and (f)) orientations at the die junction (a and b), the top of the lid (c and d) and the bottom of the PCB ((e) and (f)).

The “Underfill flux tube” parameter refers to taking into consideration or not the heat flux contraction in the calculation of the equivalent resistance of the underfill layer (Equation (3)). “Laminated substrate copper distribution” refers to the modeling of the copper distribution on the thermal properties of the substrate (Equation (5)). The parameters “Substrate core PTH”, “Substrate dielectric vias”, and “PCB thermal vias” evaluate the taking into account the presence of these structures in numerical models. When not included, a homogenized layer with uniform thermal properties was modeled. The use of empirical formulas for convection modeling and the consideration of radiation heat exchange are evaluated in the “CFD” and “Radiation” parameters, respectively. Finally, the impact of still air chamber inclination is also evaluated in the “Still air chamber inclination” parameter. The impact of all these parameters on the temperature was evaluated at different locations (junction, top lid, bottom PCB and corner PCB) and in the two configurations (horizontal and vertical orientations).

Table 4. List of parameters.

Parameters	Nominal	Variation
Lid conductivity	385 W/mK	+10%
TIM thickness	30 μm	+10%
TIM conductivity	2.6 W/mK	+10%
Underfill conductivity	0.65 W/mK	+10%
Underfill flux tube	On	On - off
Substrate thermal resistance	0.022 K/W	+10%
Laminated substrate copper distribution	On	On - off
Substrate core conductivity	0.8 W/mK	+10%
Substrate core PTH	On	On - off
Substrate dielectric conductivity	0.49 W/mK	+10%
Substrate dielectric vias	On	On - off
BGA conductivity	57 W/mK	+10%
PCB thermal resistance	0.047 K/W	+10%
PCB Emissivity	0.85	+10%
PCB FR4 in-plane conductivity	0.8 W/mK	10%
PCB FR4 out-of-plane conductivity	0.25 W/mK	+10%
PCB thermal vias	On	On - off
Box emissivity	0.91	+10%
CFD	On	On - off
Radiation	On	On - off
Still air chamber inclination	0 °	$\pm 5^\circ$

8. Results and Discussions

Table 5 summarizes the sensitivity study on the parameters for 10 W of applied power. This table presents the variation of the temperature at different locations relative to the temperature at the same locations when all parameters are at their nominal value. For discrete parameters, the variation is the absolute value of the temperature difference when each discrete parameter is deactivated. For continuous parameters, the variation is the average of the absolute value of the temperature difference for each parameter set at -10% and at $+10\%$ of its nominal value.

The parameters were classified according to four categories: those that we consider negligible (maximum variation of less than 1% on the temperature at either the junction of the chip, the top of the lid, the bottom of the PCB, or the corner of the PCB); influential (variations between 1% and 5%) and critical (variations of more than 5%). Three parameters have been identified as critical: “Radiation”, “CFD” and “substrate dielectric vias”. In many thermal studies in microelectronics, radiation heat transfer is neglected because of the underestimation of its importance in the cooling of electronics. Some authors neglect its

Table 5. Summary of sensitivity study.

Parameters	Relative variation of temperature								
	Horizontal Orientation				vertical Orientation				
	Die junction center	Lid top center	PCB bottom center	PCB bottom corner	Die junction center	Lid top center	PCB bottom center	PCB bottom corner down	PCB bottom corner up
Radiation	42.1%	42.3%	49.4%	80.6%	42.7%	43%	49.8%	65.7%	97.6%
CFD	8.6%	8.7%	8.5%	12.6%	9.4%	9.5%	10.2%	5.8%	25.7%
Substrate dielectric vias	5.4%	5.4%	1.4%	0.4%	5.6%	5.6%	1.3%	0.3%	0.3%
Substrate core PTH	2.4%	2.4%	0.7%	0.07%	2.5%	2.5%	0.7%	0.1%	0.2%
PCB thermal resistance	2%	2%	2.2%	1.8%	1%	1%	1%	5.2%	1.8%
PCB Emissivity	1.9%	1.9%	2.3%	2.9%	1.5%	1.5%	1.8%	2.2%	3.4%
Substrate thermal resistance	1.5%	1.5%	0.8%	0.3%	1.5%	1.5%	0.8%	0.2%	0.04%
PCB FR4 vertical conductivity	0.7%	0.7%	0.3%	0.03%	0.7%	0.7%	0.3%	0.02%	0.1%
Still air chamber inclination	0.7%	0.7%	0.3%	3.6%	0.04%	0.04%	0.05%	0.06%	0.2%
Laminated substrate copper distribution	0.4%	0.4%	0.4%	0.05%	0.4%	0.4%	0.5%	0.1%	0,01%
Substrate dielectric conductivity	0.4%	0.4%	0.03%	0.01%	0.4%	0.4%	0.1%	0.1%	0.02%
Lid conductivity	0.3%	0.3%	0.01%	0.05%	0.26%	0.29%	0.13%	0.03%	0.02%
Substrate core conductivity	0.2%	0.2%	0.01%	0.04%	0.2%	0.2%	0.01%	0.01%	0.03%
Box emissivity	0.2%	0.2%	0.2%	0.4%	0.3%	0.3%	0.3%	0.6%	0.6%
PCB FR4 in-plane conductivity	0.1%	0.1%	0.12%	0.07%	0.10%	0.10%	0.12%	0.07%	0.01%
TIM thickness	0.1%	0%	0.03%	0.01%	0.07%	0.02%	0.03%	0.01%	0%
BGA conductivity	0.1%	0.1%	0.03%	0.04%	0.03%	0.03%	0.01%	0.01%	0.01%
PCB thermal vias	0.1%	0.1%	0.2%	0.01%	0.01%	0.01%	0.16%	0.04%	0.2%
TIM conductivity	0.01%	0.01%	0.01%	0%	0.04%	0.01%	0.03%	0.03%	0.05%
Underfill conductivity	0.01%	0.01%	0.05%	0.02%	0.01%	0%	0.04%	0.05%	0.05%
Underfill flux tube	0.01%	0.01%	0.05%	0.02%	0.01%	0%	0.04%	0.05%	0.05%

importance in conditions where the difference in temperature is small enough to simplify their analysis. In our setting, this would lead to errors of more than 40% at the junction of the chip and up to 80% at the corners of the test card because of its high emissivity (0.85). For a more detailed investigation on the importance of radiation heat transfer in simulations, the contribution of radiation compared to that of convection in natural convection heat transfer as a function of the power dissipated in the horizontal and vertical configurations is shown in **Figure 6** and **Figure 7**.

It can be seen in both the horizontal and vertical configurations that the radiation heat transfer is responsible for more than half of the total heat flux dissipated, especially at the lower power levels, where up to 60% of the heat can be dissipated by radiation. Radiation heat transfer is therefore very important in natural convection cooling and must not be neglected.

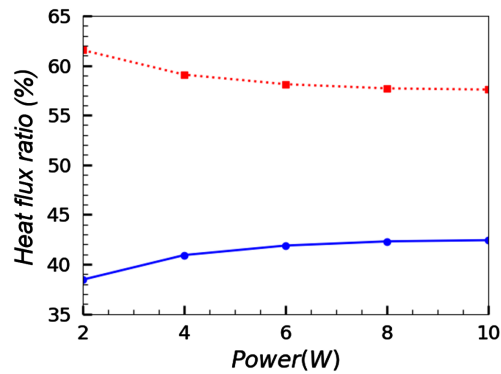


Figure 6. Contribution of radiation (dotted line) and convection (solid line) in natural convection heat transfer according to the power dissipated, in the horizontal configuration.

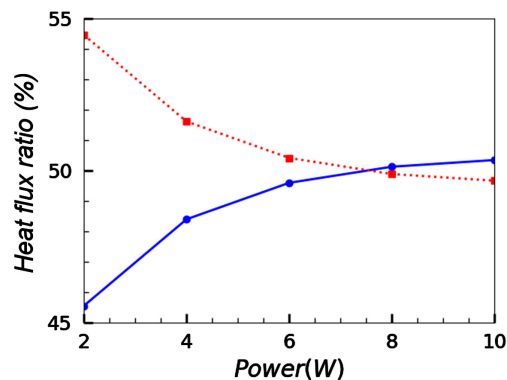


Figure 7. Contribution of radiation (dotted line) and convection (solid line) in natural convection heat transfer according to the power dissipated, in the vertical configuration.

Also, using empirical formulas to calculate convection and radiation heat transfer coefficients leads to errors of more than 8% at the junction of the chip and up to 25% at the corners of the test card in the vertical configuration. The approximations introduced by the empirical relations (for example, neglecting the non-uniformity of the velocity on the interfaces) can explain these errors. In this regard and in order to better understand the differences in temperatures agreement between the CFD and the empirical relations method, a comparison between their corresponding heat transfer coefficients has been performed in references [10] [11]. This showed that using CFD to find realistic convection coefficients is necessary to provide an accurate estimate of the temperature in the microelectronic packages.

In our previous studies [10] [11], we have shown that in natural convection most of the heat flow passes through the PCB. The vias in the substrate dielectric layers act as thermal bridges between the substrate and the PCB. Not including them in the thermal simulations leads to significant errors, about 5% at the junction of the chip. The presence of the vias in the substrate dielectric layers results in an increase by 2.25 times of the effective conductivity of the dielectric.

Four parameters were found to be influential (variation between 1% and 5%). Like the vias in the dielectric layers, the PTH in the core layer of the substrate

also plays the role of thermal bridges. Their presence leads to an increase by 3 times on the effective conductivity of the substrate core. The thermal resistances of the substrate and of the PCB also had an impact on the validity of the simulations results. As shown above, radiation is important in natural convection heat transfer, as confirmed by the impact of the PCB Emissivity. It can be concluded that a good characterization to find their precise values is necessary for these four parameters.

Negligible parameters (variation less than 1%) include the copper distribution in the substrate, the inclination of the still air chamber, the thermal vias in PCB (~0.7% of the PCB thermal resistance), the thermal conductivity of the dielectric layers, core layer, lid, underfill, BGA layer, layers of FR4 in the PCB, and the thickness and thermal conductivity of the TIM, as well as the emissivity of the still air chamber (which has a temperature that is close to ambient). Not taking them into account or varying their nominal value up to 10% did not affect much the accuracy of our simulations.

9. Conclusions

An accurate estimate of the temperature field, with an error of less than 1°C compared to experimental measurements for the vertical and horizontal orientations of the test vehicle, was obtained through a conjugate methodology that combines a high-resolution conduction model and a CFD-based model to more precisely simulate the natural convection and radiation heat transfers in micro-electronic packages. A sensitivity study was performed using this high precision model for various parameters. The sensitivity study has revealed that in order to have an accurate solution for the temperature field, the following features must be incorporated into the model:

Using CFD to find realistic convection coefficients: the use of empirical formulas to calculate heat transfer coefficients can lead to large errors (8% at the junction of the chip and 25% at the corners of the test card in the vertical configuration). These error results are mainly from the assumptions of a uniform velocity field, which is not observed when edge effects and fluid flow in a confined box are present.

Including radiation heat transfer: radiation can be responsible for more than half of the total heat flux dissipated in the studied natural convection cooling configuration, even at low power. In our case, almost all of the radiation heat transfer passes through the PCB (98%) because of its high emissivity (0.85), which is 17 times greater than that of the lid (0.05), and its surface which is 8 times larger than the surface of the lid. Given the importance of radiation in natural convection heat transfer, proper knowledge of the precise values of the emissivity of the PCB and the still air chamber walls is also important.

Model the vertical interconnections along the heat dissipation path: the heat being dissipated mainly through the PCB in the two orientations (86% for horizontal, 84% for vertical), the vias in the dielectric layers as well as the PTH in the substrate core play the role of thermal bridges and can increase significantly the

substrate out-of-plane conductivity.

Obtain the correct thicknesses and thermal properties for the substrate and the PCB: the thermal resistance of the substrate and of the PCB can have a significant impact on the simulation results. Variations that may come from manufacturing tolerances should be properly understood.

Other parameters could vary by up to $\pm 10\%$ or not be taken into account and not affect the calculated temperatures by more than 1%. These parameters include the copper distribution mapping in the substrate, the inclination of the still air chamber, the thermal vias in PCB, the thermal conductivity of the dielectric layers, the core layer, lid, underfill, BGA layer, layers of FR4 in the PCB, and the thickness and thermal conductivity of the TIM, as well as the emissivity of the still air chamber.

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Conflicts of Interest

The authors declare no conflicts of interest regarding the publication of this paper.

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