A Generic MEMS Fabrication Process Based on a Thermal Budget Approach

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Abstract

A modular and generic monolithic integrated MEMS process for integrating CMOS technology with polysilicon microstructures is presented. The proposed process flow is designed with an intra CMOS approach to fabricate the microstructures into trenches without the need of planarization techniques. After annealing at 1000˚C at significant period of time, it is shown that *Id-Vg* characteristics of the CMOS transistors remain almost unchanged, indicating their robustness to the intra process fabrication for the micromechanical structures. The CMOS module is designed with a 3 µm length as a minimum feature and this process results with a minimum of residual strain and stress on the micromechanical devices ($\varepsilon = 1.28 \times 10^{-4}$ and $\sigma = -21$ MPa).

Keywords

Thermal Annealing, CMOS, MEMS, Process Simulation, Surface Micromachining

1. Introduction

The MEMS (Micro-Electro-Mechanical Systems) acronym brings to mind mechanical structures of micrometric dimensions performing an electronically controlled preset function [1]. Currently MEMS (Microsystems) manufacturers offer this approach but usually sensors and/or actuators are separately fabricated and then bring to interaction with electronic circuitry (hybrid integration), and such hybrid systems show functional drawbacks mainly due to external wiring [2]. Nevertheless, MEMS is an evolving technology and involves more than mechanical structures, and also involves a wide variety of microcomponents (chemical, thermal, magnetic, mechanical, etc.) and electronic circuits. According to the nature of the microcomponents, the full potential of MEMS products has been possible only by the proper integration with a specific conditioning electronic circuit. In this sense, nowadays designers are facing different possibilities for integrating a monolithic system (combin-

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ing sensors/actuators and electronic devices on a single substrate) based on the careful selection of a thermal processing budget which could be required for the fabrication of both modules: microcomponents and (Complementary Metal Oxide Semiconductor) CMOS circuits [2]. Designers can choose Pre-CMOS, Post-CMOS and Intra-CMOS approaches. Each one of these approaches has a set of particular fabrication steps to generate integrated MEMS. The development of better integration approaches is the way to achieve a better system performance and new applications. Currently, some studies are considering that a half of all existing MEMS categories are fabricated using a monolithic integration approach, and some examples are print-heads, accelerometers, and recently frequency control [3] devices. This kind of integration offers a less expensive alternative to the reduction of parasitic elements and at the same time increases signal detection sensitivity of the conditioning circuitry. Some of the monolithic MEMS currently commercially available and that shows the aforementioned advantages are routinely produced by Analog Devices (ADXL series accelerometers and ADXRS series gyroscopes) [4] and Infineon Technologies in its KP200 series pressure sensors [5].

A generic integrated circuit process fabrication is one that can fabricate more than a single device. The CMOS technology proposed in this work is a generic one. However, specific microcomponents technology usually results quite limited by some specific applications. The goal of our MEMS technology is to develop a generic and modular process capable of integrating intelligent and varied microstructures by exploiting the fabrication sequence described in this work. Considering Pre-, Intra- and Post-CMOS, these approaches have in common that the production of the MEMS is adapted to the well developed CMOS processes. This means that the CMOS process could modify the original sequence of fabrication process in order to produce a new MEMS fabrication process. Hence, in this work critical thermal fabrication steps are discussed about the compatibility of CMOS with the microcomponents modules for the development of a generic MEMS technology.

2. MEMS Technology Considerations

The integration of a new MEMS technology is required for the design and development of systems satisfying the need of more and accurate functionality at lower cost. In this way we propose a MEMS technology for thermomechanical applications that may be developed by stages, the starting point is the development of a set of force-sensing circuits mainly composed by suspended Wheatstone bridges and chevron actuators. A long-term objective will be considering the development of a multi-purpose MEMS technology, which considers other related microcomponents. The monolithic integration approach will be developed considering a Polysilicon surface micromachining module and a CMOS module, whose integration is designed considering (0 0 1), 6-inch diameter, silicon wafers.

The surface micromachining module was already developed, and uses polysilicon (Poly) films as structural materials. Such module offers two structural levels, phospho-silicate glass (PSG) films as sacrifice material, and aluminum films for interconnections [6]. The chevron actuators are energy-supplied with a 15 volts source. The Poly films are also used as gate electrode for MOSFET's, thermomechanic devices [7] and piezo-resistor structures for piezo-resistive sensing force circuits [8].

The CMOS module is under development; with the purpose of fabricate digital circuits with 3μm-length as minimum feature and ±5 supply voltage. For matching the threshold voltage transistors, a twin-well diffusion and latch up-free structure were designed [9]. Finally, a polysilicon gate is proposed and no chemical-mechanical polishing (CMP) technique is considered. Next each module is discussed.

2.1. Microstructures Module: PolyMEMS INAOE Technology.

Using the PolyMEMS INAOE technology®, several static and dynamic microcomponents have been fabricated [6]. This technology uses Poly films as structural material and the electrical and mechanical properties are closely controlled by means of thermal processing conditions. Considering integration purposes and because of possible mechanical parameters variations, it is critical the close knowledge of the temperature dependence on Poly properties. This will allow the design and implementation of long-term stable micro actuators in systems with specific applications. The details of the Microstructure module can be found in [6], some highlights of it are described below:

Then, a systematic analysis about the residual stress on the 2.0 μm-thick Poly films is performed. Poly films were doped during 70 minutes at 1000˚C [8]. Moreover, the residual stress is analyzed under the influence of an additional thermal treatment in nitrogen ambient, during 30 minutes, at 1000˚C. In the PolyMEMS INAOE module,

this second thermal treatment is used to achieve a reflow of the PSG film (RPSG). In this regard, it is known that after depositing and thermal doping the Poly films, if the film is subsequently annealed, some additional crystallization could be promoted, hence a longer time annealing could lead to a residual stress decreasing [10]-[12].

According to the thermal load for the poly films, we took the Young modulus E = 154 GPa [13], then for the only-doped (single thermal treatment) poly films the residual strain and stress were $\varepsilon = 4.94 \times 10^{-4}$ and $\sigma = -79\ MPa$ (compressive) respectively. For the samples with an extra annealing treatment both parameters change to $\varepsilon = 1.28 \times 10^{-4}$ and $\sigma = -21\ MPa$ respectively, which shows a very low compressive residual stress, according to that stated in the literature [14]. After second thermal treatment the poly films shows high stability and low residual stress if these films are processed at 1000˚C. This structural equilibrium for Poly films must be kept after the overall development of the full CMOS module.

In **Figure 1**, some microcomponents fabricated with the PolyMEMS INAOE Technology are shown. **Figure 1(a)** shows the test chip PolyMEMS VB, which was designed with a 1.0 μm minimum feature. **Figure 1(b)** shows a Chevron actuator fabricated with 8-coupled arms, this type of Joule actuator is considered for the design of the force sensors. **Figure 1(c)** shows a lay-out of a Vernier-gauge arrangement for residual stress testing. **Figure 1(d)** shows the comb array of the Vernier-gauge arrangement. This routine inspection using a Scanning Electron Micrograph (SEM) for analysis is utilized in combination with a double clamped-arrangement, as a tool to calculate the very low compressive residual stress for the structural Poly films.

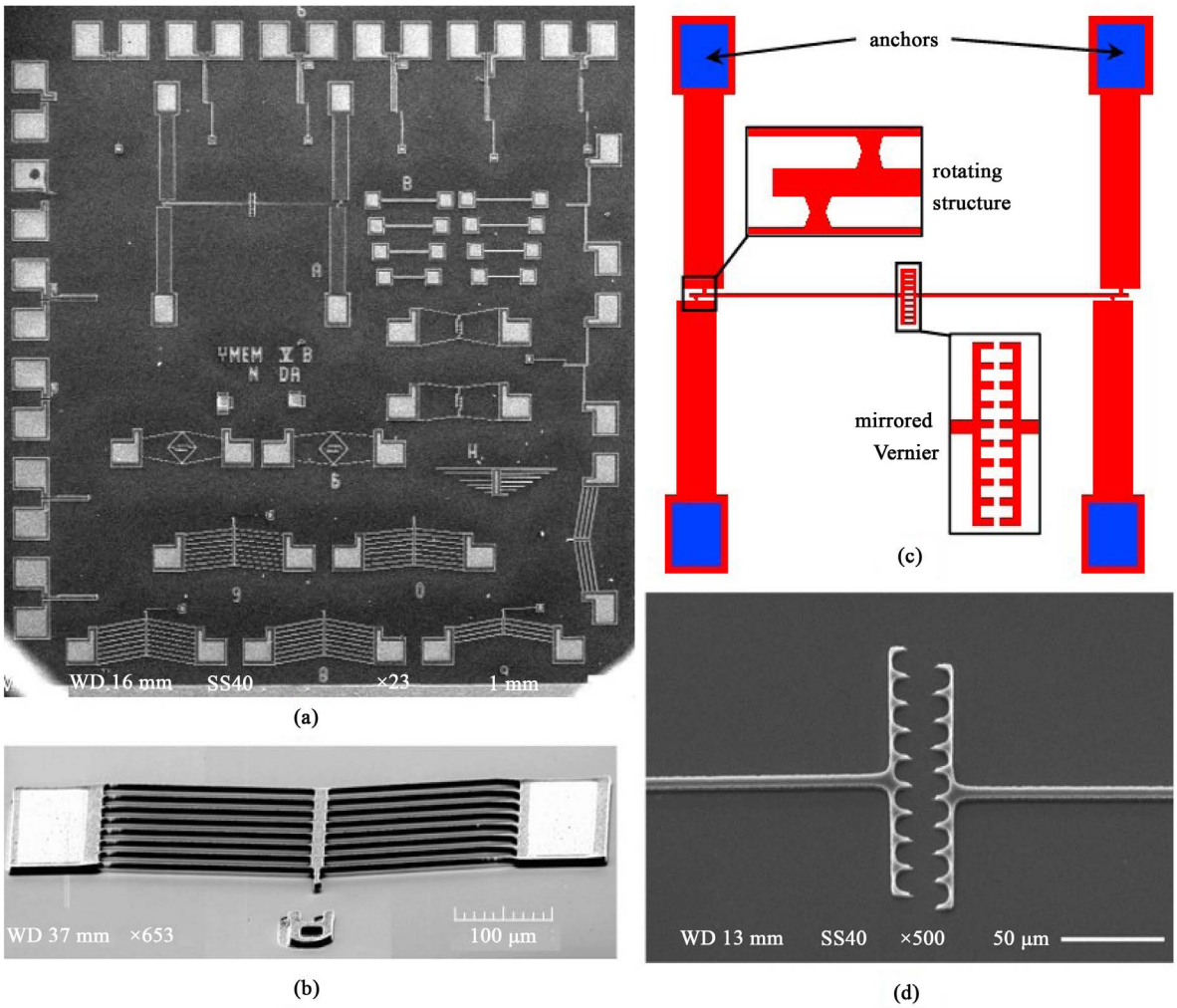


Figure 1. (a) Mechanical devices test chip for PolyMEMS technology; (b) Chevron actuator fabricated with 8-coupled arms; (c) Lay-out of a Vernier-gauge arrangement for residual stress testing; (d) Vernier-gauge, zoom in at the comb array for residual stress analysis.

2.2. MOS Module: 3 µm CMOS Technology

The CMOS module consists of 9 mask and 12 lithography steps. The main blocks are briefly discussed in the following: 10 - 20 Ω-cm (~5×10^{14} cm^{-3}), p-type, 6-inch diameter, (0 0 1) silicon wafers are selected as the substrate. Initially the formation of the N- and P- wells, as twin wells, are ion implanted and the drive-in thermal diffusion is performed at 1200˚C. The junction depth (3.5 µm) is designed to be deep enough to avoid vertical punch-trough. The active areas are defined by using Poly buffered local oxidation of silicon (PBLOCOS) for a precise feature definition. A p-channel stopper is used to reduce the spacing between devices and providing better isolation. A 200Å gate oxide is thermally grown at 900˚C in dry oxidation. 400 nm of Poly films are low-pressure chemically vapor-deposited (LPCVD) at 650˚C, after that a 1000˚C phosphorus doping is performed during 30 minutes. This process is designed with shallow source/drain junctions (0.7 µm) as well as low gate and drain/source sheet resistances to minimize the delay and increase the current drive of the devices. The titanium silicide ($TiSi_2$) electrodes are defined using a self-aligned process realized at 900˚C in nitrogen ambient. A precise low-dose of boron ions is implanted for threshold adjusting of CMOS transistors. Interconnecting aluminum film is deposited and patterned, and finally a 450˚C sintering is performed. The main process specifications are summarized in **Table 1**. **Figure 2** shows a cross section for the 3 µm CMOS cell structure obtained from a simulation of the process using the Athena environment simulation from SILVACO.

Figure 3 shows the full thermal load for the 3 µm CMOS process flow. The 1200˚C thermal drive-in for the twin-well diffusion is performed during 2 hours, any other lower temperature could lend to an unnecessary longer diffusion time.

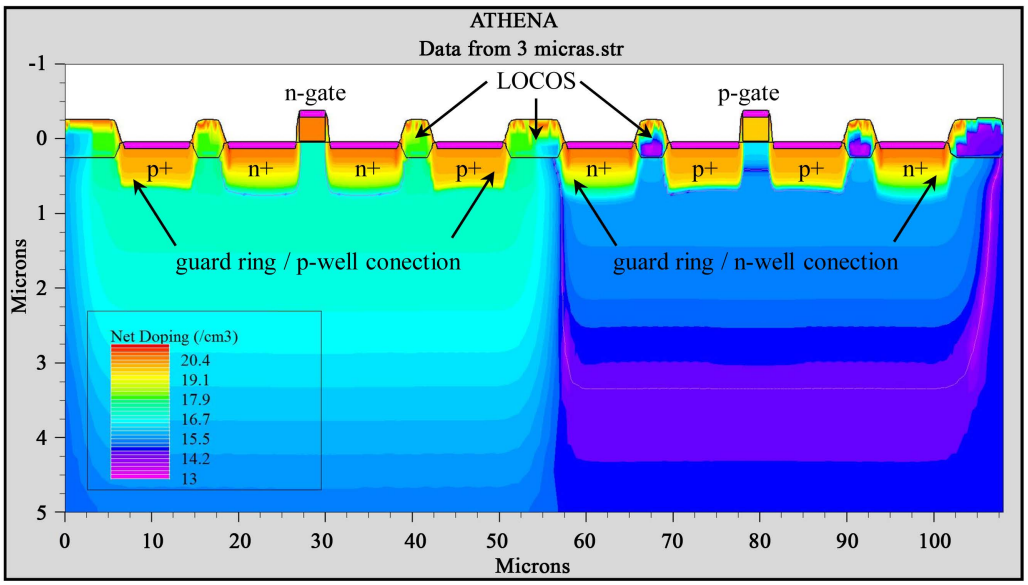


Figure 2. CMOS cell structure after full fabrication.

Table 1. CMOS Module specifications.

Parameter	Symbol	Value	Units
Threshold Voltage N/P channels	Vto	700	mV
Gate Oxide Thickness	Tox	20	nm
N-Well Depth	Xnwell	~3.5	µm
N-Well Surface Concentration	Nnwell	~4.5×10^{15}	cm^{-3}
P-Well Depth	Xpwell	~3.5	µm
P-Well Surface Concentration	Npwell	~9×10^{16}	cm^{-3}
Poly Gate thickness	Tg	0.4	µm
Source/Drain Junction Depth	Xj	0.7	µm

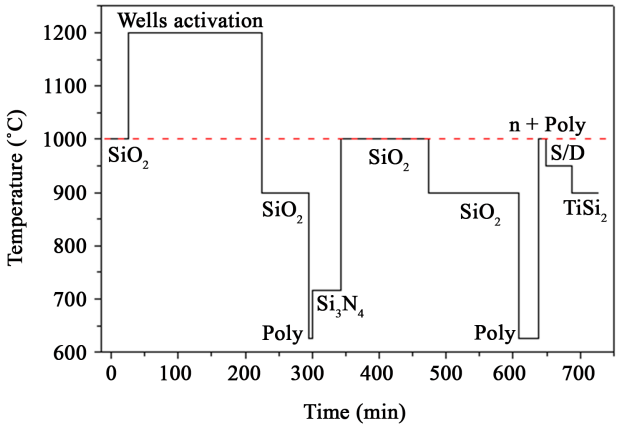


Figure 3. Thermal budget for the 3 μm CMOS process. The dashed line limits the allowed temperature for fabrication process of microstructures for an Intra-CMOS approach.

3. Integration of a MEMS Technology

Some materials and chemical ambient for full fabrication must be correlated with some type of integration approach. A Post-CMOS approach using the current PolyMEMS INAOE module cannot be compatible due to the requirements for the LPCVD Poly films, which are doped and thermally annealed at 1000˚C for a time longer than 30 minutes. The other options could be the Pre and Intra-CMOS approaches. In this sense, the PolyMEMS INAOE® technology has a thermal budget limited to 1000˚C, and according to the CMOS thermal budget shown in **Figure 3**, a Pre-CMOS approach could not be adequate. A Pre-CMOS is unsuitable due to the eventually long time increment required to adjust the twin-well drive-in from 1200˚C to 1000˚C. Given the above considerations, as alternative we are approaching to focus on the Intra-CMOS integration, keeping safe the CMOS module, since the INAOE has its own facility for device fabrication, adapt and optimize the required process flow process to minimize both electronic and mechanical degradation in accordance with the thermal budget.

3.1. Thermal Analysis on CMOS Process Design

For developing a practical intra-CMOS process, it is necessary to consider that the CMOS module is more sensitive to thermal treatments than the polysilicon microstructures. Because the goal is the integration of these different fabrication modules, a thermal study related with dopant profiles is required. For the analytical study, considering the varied CMOS doping steps and the related annealing cycles, a wide range of overall annealing time must be considered. The simulation routines were performed using SILVACO® suite that contains the Athena and Atlas environments in which the tuning of all the modules was performed with the data obtained from the characterization of the 3μm CMOS technology here developed.

For example, the final part of the CMOS module is designed with a silicon/silicide interface for electrical interconnection, which imposes limitations to the post thermal cycles to a 900˚C maximum range, for avoiding structural interface damages due to titanium silicide (TiSi2) reactivity [15]. On the other hand, at the initial part the P-N wells drive-in require a 1200˚C annealing temperature. At this high range temperature, we have identified a breaking step, where the CMOS sequence could be interrupted as a secure practical way to avoid undesirable post-thermal side effects on the CMOS structure. The full mechanical module may be fabricated after P/N well annealing and then concluding with the rest of CMOS steps without affecting the overall sequence.

As an example of our design approach, a thermal simulation was performed to demonstrate the invariance of the P/N wells (CMOS) after a long annealing time at 1000˚C as that required for the microstructure fabrication. **Figure 4** shows the simulated post-annealing effect on the P/N wells after 200, 400, 800, 1000 and 2000 minutes of thermal annealing under nitrogen ambient at 1000˚C. P- and N-well show 3.5-μm junction depth after 1200˚C annealing. **Figure 4** shows both impurity profiles and it can be seen that both remain almost unchanged with annealing time; also it is shown that both junction depths are remain at its design value, the annealing time was set with the intention to demonstrate that any type of microstructure, that may require a very long annealing time

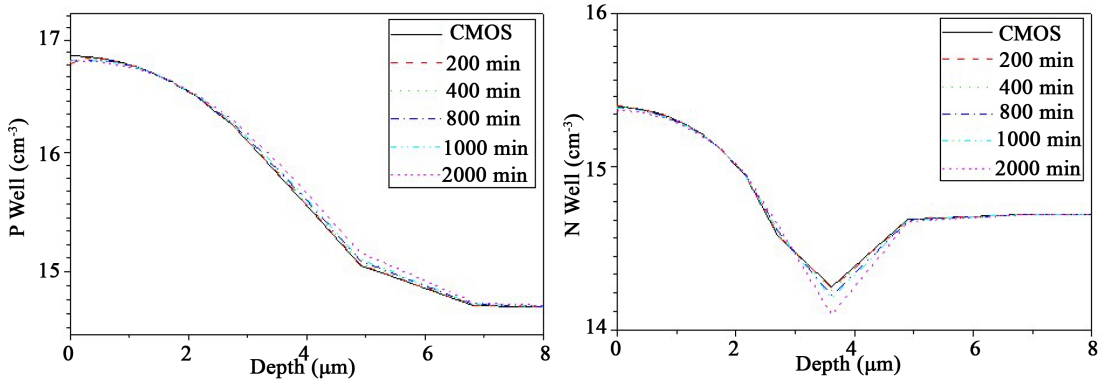


Figure 4. P-well (a) and N-well (b) junction depth under different post-annealing thermal cycles at 1000˚C.

at 1000˚C, could really be considered. The most significant issue observed after the very long post-annealing treatments, was a slight surface concentration variation at both wells, which is due to boron and phosphorus segregation at both wells/capping oxide interfaces [16].

3.2. Trench for Microstructures

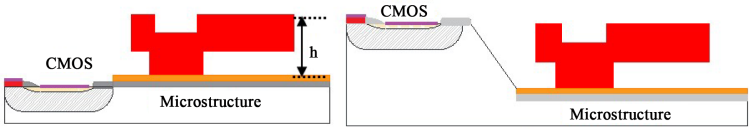
The way for the electronic-mechanical coupling is another key step in the design of the integrated process. **Figure 5(a)** shows the step height h of some poly-microstructure facing the surface CMOS diffusions. It can be observed the high aspect ratio of the microstructures. In the intra-CMOS approach, the microstructures will be fabricated before completing the CMOS steps, which means the CMOS photolithography steps will be affected by the height of the already defined microstructures. It is well known that CMOS features are directly affected by some process variations like misalignments, film thickness variations due to deposition techniques or step coverage. Our integration approach is designed to be developed without some planarization technique, hence the microstructures depicted in **Figure 5(a)** will cause some lateral size variability during the photolithography steps for developing the CMOS devices.

The M^3EMS (Modular Monolithic MEMS) technology developed at Sandia National Laboratories was one of the first demonstrations of the MEMS-first integration concept [17]. In this approach the multi-layer poly microstructures are built in a trench, which has been etched into the bulk silicon using an anisotropic wet silicon etchant. After formation of the poly microstructures, the trench is refilled with an LPCVD oxide film and planar zed with a CMP step. Subsequently, the wafer with these trenches are used as starting material in an unmodified CMOS process, then the CMOS circuitry is fabricated in areas adjacent to the trenched micromechanisms.

In our approach, we are considering the case when the microstructures are placed inside a shallow trench. In a general trace **Figure 5(b)** shows a graphical representation for this approach. In this approach the trenched microstructures result uncritical for the minimum feature definition, considering the subsequent CMOS photolithography steps and the final interconnection with the microstructures. The depth of the trench is directly related with the specific microstructure arrangement but is no deeper than 6 microns. We are using P-type and (0 0 1) silicon wafers, hence when the shallow trench is etched with aqueous Tetramethylammonium hydroxide (TMAH) the four fold symmetry wall-sloped allows the deposition of interconnecting stripes.

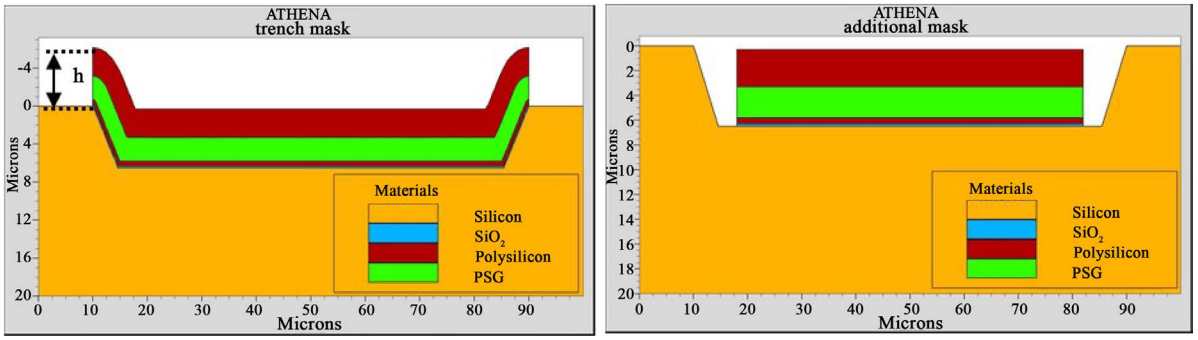
Considering general aspects for a trench some morphology requirements must be carefully considered. For example in the integration work presented in [18], which is developed by Samsung Advanced Institute of Technology (SAIT), using a Pre-CMOS approach with a trench to house the microstructures, the resulting trench shows an irregular material stacking at the edge of the trench in a similar way as that depicted in **Figure 6(a)**.

In our approach without planarization step, the presence of material stacking around the trench, similar to **Figure 6(a)**, complicates the subsequent photolithography process but also results more difficult to define geometries over the PSG at the bottom of the trench. To compensate the lack of planarization step we propose the use of an extra fabrication mask to etch the materials around the trench. By using this extra mask, the height ***h*** will disappear and both the CMOS and microstructure definition become easier. In **Figure 6(b)** a representation of this extra etching step is presented.



(a) (b)

Figure 5. Artistic view of: (a) Schematic of an integrated microstructure besides surface CMOS diffusions showing the resulting aspect ratio differences; (b) Cross section of the generic integrated MEMS process here proposed.



(a) (b)

Figure 6. Simulation of: (a) Irregular material stacking simulated according to the scheme described in [18]; (b) Material stacking using an extra photolithographic mask for etching the material around the trench.

3.3. Integration of MEMS Technology

The proposed monolithic integrated MEMS fabrication process is divided into four main sections; all the fabrication sequence is completed with 13 masks and 16 photolithography steps:

1) CMOS Part I. The process starts with an initial thin oxide (~200Å) to define the alignment marks and then the trenches are defined by using aqueous TMAH solution for CMOS compatibility. Low dose ion implantation for P and N wells and immediately a thermal drive-in at 1200˚C is performed in nitrogen ambient during 200 minutes. These steps are listed below.

	Step Process:
1.	Initial Oxidation, T = 1000˚C, dry O_2, Tox = 20 nm.
2.	Mark alignment and TMAH silicon etch at 60˚C.
3.	P implantation, Dose = 6.5×10^{10} cm^{-2}, (N-well). Energy = 100 KeV
4.	B implantation, Dose = 1.5×10^{13} cm^{-2}, (P-well). Energy = 80 KeV
5.	Drive-in at 1200˚C, 200 minutes, N2 ambient.
6.	Etching of initial oxide.

2) Poly Microstructures. An insulator film is deposited for electrical isolation between the microstructures and the surface wafer. Then a sacrificial material is deposited followed by the deposition, doping and patterning of the structural material inside the trenches. A thermal treatment is realized at 1000°C to minimize the residual stress.

	Step Process:
7.	Thermal oxide, T = 1000˚C, Tox = 0.3 µm.
8.	LPCVD intrinsic polysilicon, T = 650˚C, Tpoly = 0.5 µm.
9.	Sacrificial oxide deposition, Tox = 3.0 µm
10.	Structural material deposition, Tox = (2.0 µm)
11.	Thermal annealing at 1000˚C, t = 120 minutes in N2.

3) CMOS Part II. After the complete definition of the microstructures, the CMOS process sequence is realized in the top surface of the wafer. The standard PBLOCOS CMOS process is realized and the microstructures remain covered by the stacked materials from the local oxidation process. Field oxidation has a thermal cycle of 1000˚C for 2 hours, and serves as a stress reduction thermal cycle for the microstructures. The following fabrication sequence is listed below.

	Step Process:
12.	PBLOCOS. Deposition of a stacked silicon dioxide, polysilicon and nitride films.
13.	Active area definition.
14.	Channel stopper implantation
15.	Field oxide growing at 1000˚C. Tox = 0.58 μm, t = 2 hours
16.	VTn boron adjust implantation
17.	VTp boron adjust implantation
18.	Gate oxide T = 900˚C, Tox = 20 nm.
19.	LPCVD Gate Poly, Tpoly = 400 nm
20.	Poly phosphorus doping at 1000˚C, 10 Ω/□
21.	Source/Drain implantation
22.	Dopant activation at 950˚C.
23.	Titanium Salicidation at 900˚C

4) Interconnections and Releasing. The passivation layer is deposited to protect both the CMOS and microstructures devices. The interconnection between the CMOS and the microstructures is carried out in the metallization step by using a sputtered aluminum film to ensure proper step coverage from the top of the wafer (CMOS area) to the bottom of the trench (microstructure area). The final step in the fabrication process is the sacrificial etch to release the microstructures. The last etching process depends on the specific microstructure geometries, and it can be done by some dry or wet etching technique.

	Step Process:
24.	Passivation film deposition.
25.	Contact definition and etching
26.	Aluminum deposition and patterning (simultaneous interconnection)
27.	Sintering at 450˚C (gas forming)

Figure 7 shows a cross-section of the simulated MEMS fabrication process; inside the trench are the main devices for this technology.

4. Discussion of Final Thermal Annealing

Figure 8 shows the simulated drain current (I_d) versus gate voltage (V_g) curves for the discrete CMOS transistors and the change in I_d current after annealing of the devices at 1000˚C at different period of time. It can be seen that *Id-Vg* characteristics of the transistors remain almost unchanged, indicating their robustness to the intra process fabrication of the micromechanical structures. The current in **Figure 8** is displayed for a W/L of 1/3, in other words a unitary transistor. In order to demonstrate the endurance of the CMOS process to the thermal treatments needed for completion of the MEMS fabrication, **Figure 9** shows the impact of the annealing time on the threshold voltage of the devices.

Figure 10 shows the simulated drain current (I_d) versus drain voltage (V_d) curves at different gate voltage, for

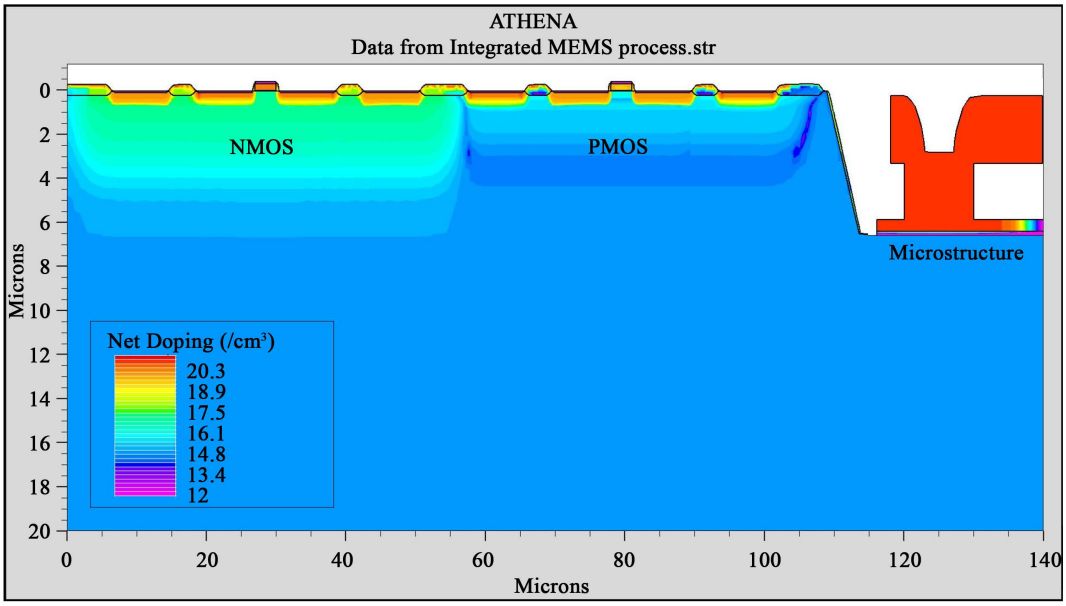


Figure 7. Cross-section view of the proposed integrated MEMS technology.

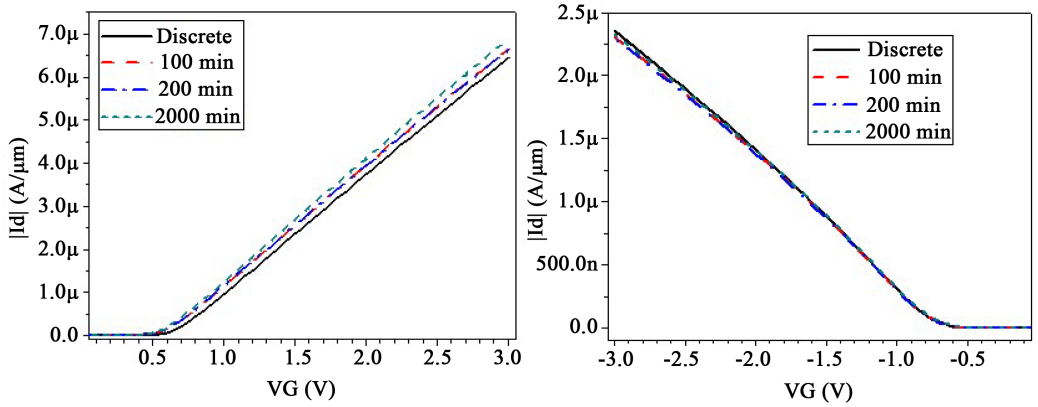


Figure 8. Simulated Vg vs. Id curves for discrete transistors and after three additional thermal cycles. (a) NMOS transistors and (b) PMOS transistor. Both curves are normalized with the width (1 µm) and the length is the minimum feature (3 µm).

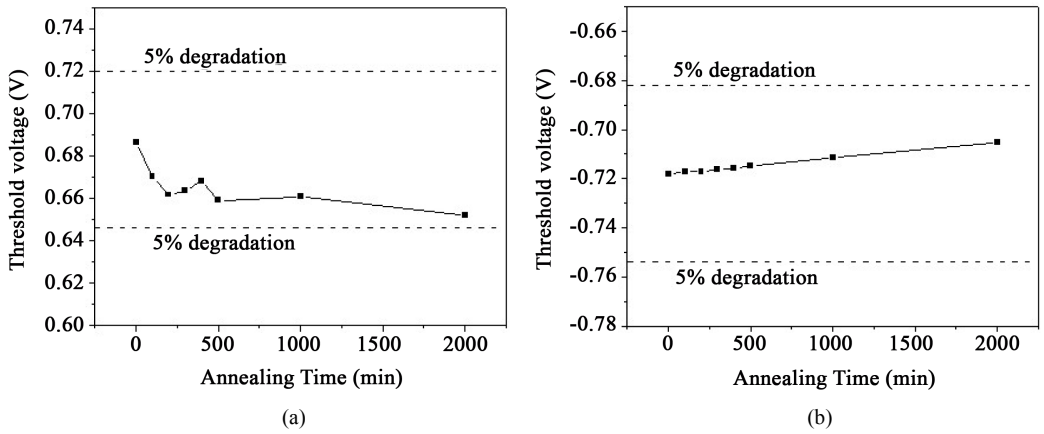


Figure 9. Threshold voltage variations on CMOS transistors, after annealing time at 1000˚C. (a) NMOS; (B) PMOS.

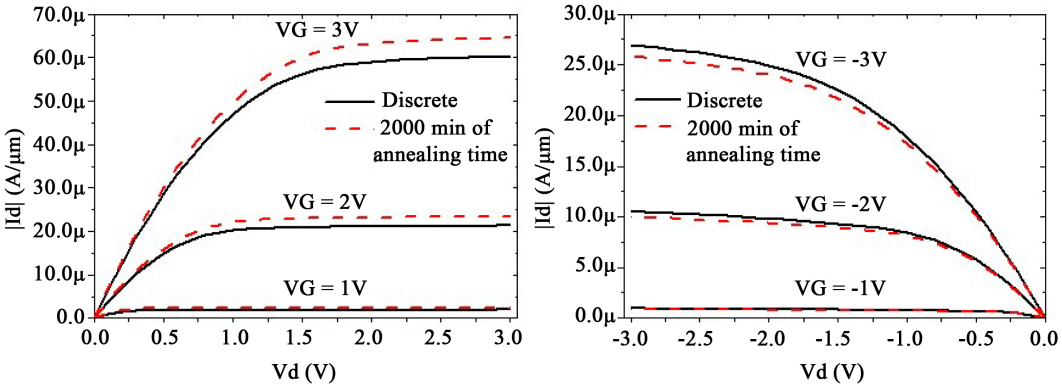


Figure 10. Simulated I_d vs. V_d curves for discrete transistors and after a 2000 minutes of annealing. (a) NMOS transistors and (b) PMOS transistor. The voltage values V_g are fixed at 1, 2 and 3 volts.

discrete transistors and after 2000 minutes of annealing time. The slight variations for the drain current I_d are corresponding with the graphs shown in **Figure 8** and **Figure 9**, such Id variations are attributed to the slight variations on the surface dopant concentration of the P/N wells/oxide interfaces previously analyzed in **Figure 4**. The overall result is that the CMOS devices and microstructures can be fabricated on the same substrate with minimal variation in the electronic-mechanical performance after 2000 minutes of annealing time.

5. Conclusion

A generic and modular design approach for a monolithic MEMS process is proposed without the need of any planarization techniques. The integration is realized with CMOS devices and polysilicon microstructures. From the simulation results, it can be concluded that a non-significant degradation on the CMOS performance devices is observed after MEMS fabrication. The intra process approach showed in this case, to be the best approach for a modular design of a MEMS fabrication process. The thermal budget of the modules plays a crucial role, because it sets the conditions for obtaining the complete set of devices fabricated near their optimal point, that is, without degradation of current handling and without Vto shift in the CMOS process and with the minimum residual stress on the micromechanical devices.

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