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Characterization and Modeling of 22 nm FDSOI Cryogenic RF CMOS

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ABSTRACT Analog and RF mixed-signal cryogenic-CMOS circuits with ultrahigh gain-bandwidth product can address a range of applications such as interface circuits between superconducting (SC) single-flux quantum (SFQ) logic and cryo-dynamic random-access memory (DRAM), circuits for sensing and controlling qubits faster than their decoherence time for at-scale quantum processor. In this work, we evaluate RF performance of 18 nm gate length (L_G) fully depleted silicon-on-insulator (FDSOI) NMOS and PMOS from 300 to 5.5 K operating temperature. We experimentally demonstrate extrapolated peak unity current-gain cutoff frequency (f_T) of 495/337 GHz (1.35×/1.25× gain over 300 K) and peak maximum oscillation frequency (f_{MAX}) of 497/372 GHz (1.3× gain) for NMOS/PMOS, respectively, at 5.5 K. A small-signal equivalent model is developed to enable design-space exploration of RF circuits at cryogenic temperature and identify the temperature-dependent and temperature-invariant components of the extrinsic and the intrinsic FET. Finally, performance benchmarking reveals that 22 nm FDSOI cryogenic RF CMOS provides a viable option for achieving superior analog performance with giga-scale transistor integration density.

INDEX TERMS 22 nm fully depleted silicon-on-insulator (FDSOI) technology, cryogenic-CMOS, cut-off frequency (f_T), maximum oscillation frequency (f_{MAX}), quantum processor, small-signal-equivalent circuit model.

I. INTRODUCTION

CRYOGENIC superconducting (SC) digital processors operating at 4 K, employing Josephson junctions (JJs) for single flux quantum (SFQ) logic, offer the promise of greatly reduced operating power for high-performance cloud computing systems due to the exceptionally low energy per operation of SFQ circuits [1]. This allows a significant reduction in overall energy delay product and hence has led to renewed interest in SC computing with SFQ. It is equally important to complement SC logic technologies with a compatible high-bandwidth, low latency memory technology co-located in the same 4 K temperature plane. For instance, the operation of a 1.3 GHz embedded cryo-dynamic random-access memory (DRAM) macro with a 2T-gain-cell was demonstrated at 4 K as an option for ultrahigh density cryo-memory sub-system for SFQ logic processors [2]. Integration of cryogenic-DRAM in the same thermal plane as the JJ SC logic shortens the interconnect length and improves data access latency. Reduced sub-threshold leakage through the DRAM access transistor at cryogenic temperature was harnessed to enable $10^6\times$ higher retention time and consequently lower refresh power [2]. Memory capacity of cryogenic-DRAM can further be increased by designing the DRAM memory cell at denser CMOS nodes. Interfacing cryogenic DRAM with SC logic still remains a technology challenge. For instance, SFQ logic operates with 2 mV amplitude pulses with picosecond duration which implements input and output circuits challenges. Also, JJs by themselves cannot directly drive bit/wordline or CMOS sense amplifiers in DRAM arrays, which operate at 0.8 to 1 V supply. In this context, multistage signal booster and level translator circuits with high gain (400 V/V) and GHz bandwidth, are required to interface SC circuits with cryo-DRAM memory.

Furthermore, cryogenic-CMOS based analog and mixed-signal interface systems have been proposed for control and read out of qubits in a large-scale quantum computer [3]. Placing the cryo-CMOS control electronics in close physical proximity to the quantum processor can provide significant benefits in terms of system scalability and low latency [4]. As the cryogenic qubit controller requires generation and acquisition of GHz range signals with low power dissipation and high immunity to noise [5], design-space exploration

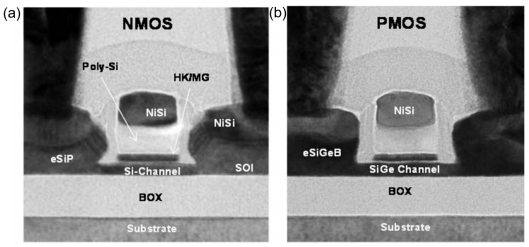

FIGURE 1. Schematic of device structure and xTEM image of regular-well 22 nm FDSOI for (a) and (c) Si nFET and (b) and (d) SiGe pFET respectively, as shown in [6].

of cryogenic RF circuits is required to ensure strict power budgets along with superior analog and RF performance.

The ultra-thin body and buried-oxide (UTBB) fully depleted silicon-on-insulator (FDSOI) CMOS platform is a potential platform for both of the above-mentioned cryogenic RF applications, due to high transistor density, low power dissipation, and reduced parasitic and optimized RF performance [6], [7]. Commercially available FDSOI CMOS technologies (22 and 28 nm node) have been investigated in detail down to 4.2 K, along with self-heating effects [8] and device variability [9]. However, these studies mainly evaluated the temperature dependence of MOSFET dc parameters, like threshold voltage, sub-threshold swing, transconductance, and drive-current. RF performance of both FDSOI NMOS and PMOS has not been yet studied in detail and quantified at a deep cryogenic temperature [10]. In addition, small-signal circuit models for cryogenic FDSOI are also essential to develop a reliable RF circuit design toolkit, which is still not in existence for 22 nm cryogenic FDSOI technology [11].

This work presents a detailed description and analysis of RF performance gain in 22 nm FDSOI technology at cryogenic temperature, as demonstrated in our previous work [12]. In this article, we investigate RF performance Si NMOS and SiGe PMOS [6] FETs at cryogenic temperature on Globalfoundries 22 nm FDX CMOS platform. Electrical dc and RF characterization of 22 nm FDSOI FETs were performed from 300 K down to 5.5 K. RF FoM such as transistor cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}) were extracted as a function of drain current (I_{DS}) bias and operating temperature. A small-signal equivalent circuit of MOSFET [13] was utilized to model the RF response of FDSOI FET from 300 to 5.5 K. Temperature variation of the small-signal equivalent model parameters was used to identify the temperature-dependent and temperature-invariant FET parameters that set the limit of cryogenic RF performance. Finally, the performance of 22 nm FDSOI FETs at cryogenic temperature is benchmarked against other advanced node cryogenic CMOS technologies.

II. DEVICE DESCRIPTION AND EXPERIMENTAL DETAILS

Commercially available 22 nm FDSOI CMOS technology provides Si channel nFET and SiGe channel (with Ge content around 25%) pFET fabricated with gate-first high-k metal gate process [6]. Fig. 1 shows xTEM of 22 nm FDSOI Fig. 1(a) and (c) nFET and Fig. 1(b) and (d) pFET, respectively. The thickness of the un-doped ultra-thin semiconductor channel is about 6 nm, while the buried oxide is 25 nm thick. Capacitance equivalent thickness (CET) of the high-k gate-stack was found to be 1.3 nm. In this work, experimental measurements were performed down to 5.5 K using Lakeshore CPX-VF cryogenic probe station. Cryogenic dc characterization was performed using a Keithley 4200 SCS parameter analyzer, whereas the RF measurement setup consists of ground–signal–ground (GSG) probes with 50 μm pitch and an 8722D vector network analyzer. S-parameters are measured from 300 to 5.5 K, on 18 and 28 nm LG FETs with 16 gate-fingers of 0.5 μm width each, over 0.5–35 GHz frequency range, under cold-FET (VDS = 0 V, |VGS| = 0, 0.2 V) and saturation (|VDS| = 1.0 V, |VGS| = 0.0–1.2 V) bias conditions. S-parameters of the ON-chip open and short structures are also measured for all temperatures. A two-step de-embedding method using the ON-chip open and short structures, as described in [14], has been followed to correct for the interconnect-line and access parasitic embedded in the test structure. S-parameters measured on the open structure were converted to Y parameters (Y_{Open}); this provides the parallel-connected pad and interconnect parasitic. Similarly, the S-parameters of the short structure were measured and converted to Y parameters (Y_{Short}). The series components of the interconnect parasitic were then obtained from the open and short measurements by $Z_{Series} = (Y_{Short} - Y_{Open})^{-1}$, as described in [14]. Finally, the transistor Y-parameters were obtained by measuring the transistor S-parameters, converting them to Z-parameters (Z_{DUT}), and sequentially de-embedding both series and parallel parasitic, using

$$Y_{Transistor} = \left((Z_{DUT} - Z_{Series})^{-1} - Y_{Open}\right) \quad (1)$$

where, Z_{DUT} is the Z-parameter representation of the measured device. These de-embedded transistor Y-parameters were then used to extract the RF FoMs of the transistor, such as f_T and f_{MAX}.

Pad and access parasitic de-embedded S-parameters were then used to extract the RF FoMs of the transistor, such as f_T and f_{MAX}. Subsequently, "cold" FET measurement at $V_{GS} = 0$ V was employed for both gate length structures to further de-embed the effect of extrinsic FET resistances [15]. Extrinsic FET capacitances were also de-embedded using the "cold" FET measurements in accumulation condition (at $V_{GS} = -0.2/+0.2$ V for nFET/pFET), as explained in [15]. Finally, access and extrinsic FET parasitic de-embedded S-parameters were used to extract the intrinsic FET parameters at each bias point from the measurements in saturation condition.

III. RESULTS AND DISCUSSIONS

A. CRYOGENIC DC CHARACTERIZATION OF 22 nm FDSOI

The well-tempered transfer characteristics (I_D–V_{GS}) of 18 nm gate length (L_g) nFET and pFET from 300 K down to 5.5 K, are shown in Fig. 2(a) and (b) for linear ($V_{DS} = 50$ mV) and

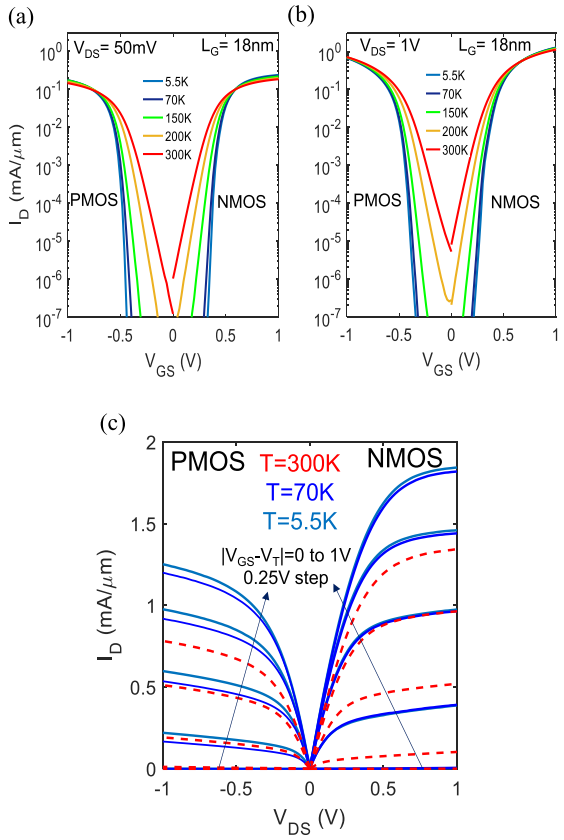

FIGURE 2. Transfer characteristic of 22 nm FDSOI nFET and pFET (L_G = 18 nm) from 300 to 5.5 K in (a) linear (V_{DS} = |50 mV|) and (b) saturation (V_{DS} = |1 V|) region. (c) Output characteristic of nFET and pFET (L_G = 18 nm) at 300, 70, and 5.5 K.

saturation region ($V_{DS} = 1$ V), respectively. The output characteristics with excellent saturation behavior [see Fig. 2(c)] shows drain current (I_{DS}) improvement of 37% for nFET and 60% for pFET under iso-gate overdrive ($|V_{GS} - V_{T,Lin}| = 1$ V) at 5.5 K compared to 300 K. The linear ($V_{TH,Lin}$) and saturation ($V_{TH,sat}$) region threshold voltage increase at cryogenic temperature for both nFET and pFET [see Fig. 3(a) and (b)], due to the increase in the Fermi-potential at lower temperature [16]. $V_{TH,Lin}$ shift in SiGe pFET (160 mV) was found to be more compared to Si nFET (122.5 mV) at 5.5 K. However, the FD-SOI technology harnesses the back-gate biasing capability even at cryogenic temperature, which can be exploited to re-target the V_{TH} at low temperature. Fig. 3(c) shows the V_T tuning capability of the n-FDSOI MOSFET at different temperatures. Back-bias voltage (V_B) of +2 V is required to re-target the V_{TH} at 5.5 K to that at 300 K for 18 nm NMOS FDSOI FETs. Interestingly, the back-biasing efficiency ($\gamma = \Delta V_T/\Delta V_B$) of n-FDSOI FETs was found to be constant across temperature ($\gamma = -80$ mV/V). This indicates the highly doped p-well substrate does not undergo dopant freeze-out even at 5.5 K. Subthreshold slope (SS), on the other hand, improves for both the NMOS and PMOS down to cryogenic temperature [see Fig. 3(d)]. However, SS does not scale linearly with temperature below 70 K and saturate around 20 mV/dec. This can be attributed to the location of the Fermi-level close to the high interface trap density (D_{it}) region, as well as a sharp change in Fermi occupation function at cryogenic temperature, both leading to higher interface trap response capacitance (C_{it}) [17]. This results in a sharp rise in the n-factor ($n = SS_{Experimental}/SS_{Ideal}$) below 70 K with an inverse temperature dependence (T^{-1}), as shown in the inset of Fig. 3(d). The transconductance in the saturation region ($g_{m,sat}$) is plotted as a function of the gate length (L_G), in Fig. 3(e) and (f) for nFET and pFET, respectively. $g_{m,sat}$ scales as $L_G^{-0.3}$ for both deeply scaled ($L_G < 50$ nm) nFET and pFET across all temperatures. Improvement in $g_{m,sat}$ was found to be 33%/25% for nFET/pFET from 300 to 5.5 K, across all channel lengths, due to reduced phonon scattering and improved source/drain contact resistance [12]. However, boost in $g_{m,sat}$ is saturated below 150 K as carrier transport is dominated by temperature invariant surface roughness (SR) scattering. Also, it should be noted that, $g_{m,sat}$ in nFET FDSOI was found to saturate below 28 nm gate length, whereas it continues to improve with L_G scaling in pFET FDSOI. This can be possibly due to the fact that $g_{m,sat}$ at scaled gate length nFET is still dominated by the n+ Si source/drain contact resistance. However, this is not the case for Si-Ge channel PMOS since the source/drain contact resistance of p+ SiGe is lower compared to NMOS.

B. CRYOGENIC RF CHARACTERIZATION OF 22 nm FDSOI

Cryogenic RF characterization of 22 nm FDSOI technology involves extraction of two main RF FoMs as a function of drain current bias and operating temperature, namely transistor cut-off frequency (f_T) and maximum oscillation frequency (f_{MAX}). In order to extract f_T and f_{MAX}, access parasitic de-embedded S-parameters were used to calculate short-circuit current gain (H_{21}) and Mason's unilateral power gain (U), as mentioned in [10]. f_T was calculated through −20 dB/dec extrapolation of H_{21} to unity gain ($|H_{21}| = 0$ dB), over a frequency range of 1–20 GHz. Fig. 4 shows the measured $|H_{21}|$ (symbols), under peak-g_m gate bias and $|V_{DS}| = 1$ V, along with −20 dB extrapolation (line) for NMOS (red) and PMOS (blue) at 300, 70, and 5.5 K in Fig. 4(a)–(c), respectively. A similar method was followed to extrapolate f_T as a function of drain-current bias. Fig. 5(a) and (b) plot the drain-current dependence of extrapolated f_T for different temperatures ranging from 300 to 5.5 K for NMOS and PMOS, respectively. Extrapolated peak-f_T as a function of temperature shows an improvement of 35% from 367 GHz at 300 K to 494 GHz at 5.5 K for NMOS and 25% from 268 GHz at 300 K to 337 GHz at 5.5 K for PMOS, as shown in Fig. 5(c).

Similarly, −20 dB extrapolation of |U| to unity power gain ($|U| = 0$ dB) allows extraction of f_{MAX}. Fig. 6 plots measured |U| (symbols), under peak-g_m gate bias and $|V_{DS}| = 1$ V, along with −20 dB extrapolation (line) for NMOS (red) and PMOS (blue) at 300, 70, and 5.5 K in Fig. 6(a)–(c), respectively. Drain current bias dependence of extrapolated f_{MAX} across temperature is also extracted for NMOS [see

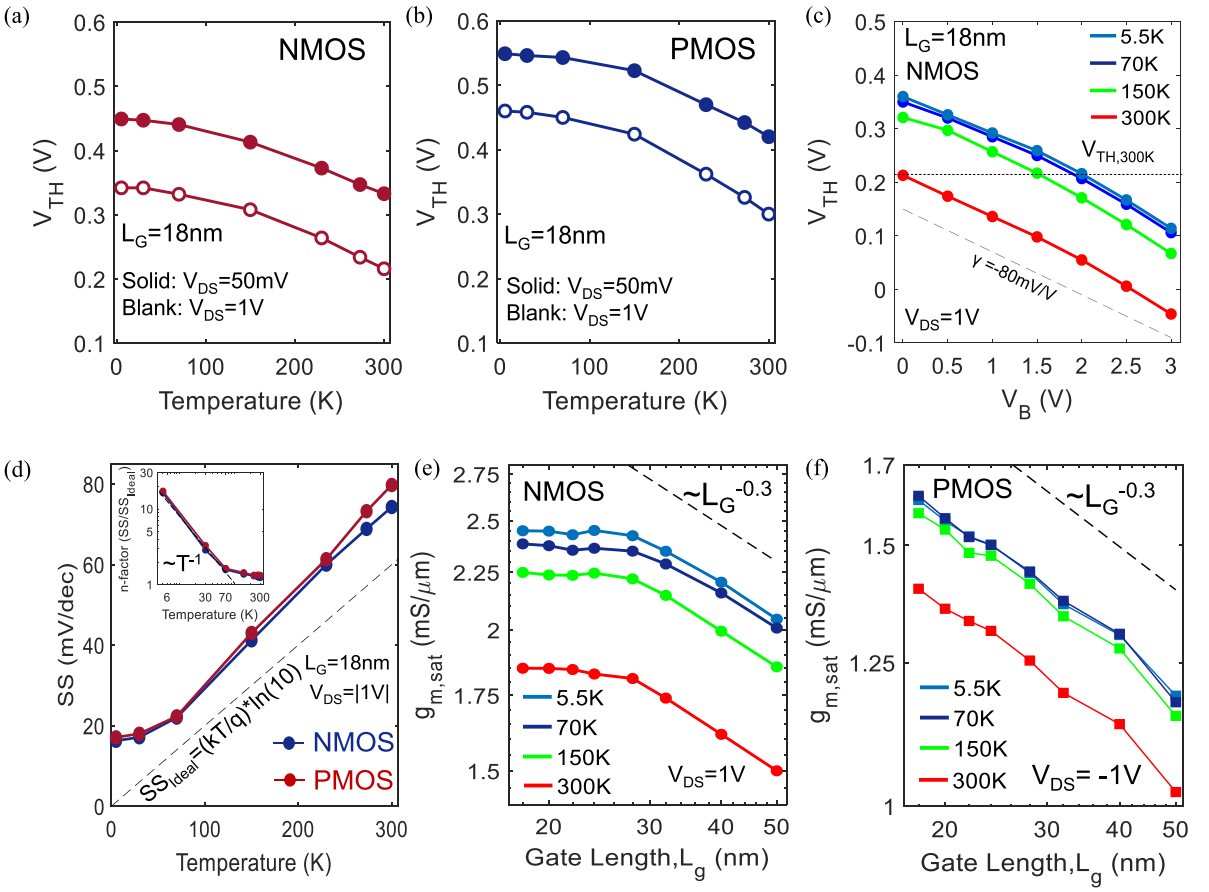

FIGURE 3. **DC characterization of cryogenic FDSOI technology. Threshold voltage shift with temperature at $|V_{DS}| = 50$ mV and $|V_{DS}| = 1$ V for (a) nFET and (b) PMOS; (c) 200 mV negative shift in V_{TH} can be obtained through back-bias at 5.5 K to match the same V_{TH} at 300 K. (d) SS at $|V_{DS}| = 1$ V for NMOS (blue) and PMOS (red), n-factor ($n = SS/SS_{Ideal}$) increase sharply with inverse temperature dependence at cryogenic regime (inset), due to high interface trap response capacitance (C_{it}); L_G scaling trend of transconductance ($g_{m,sat}$) at different temperatures (300, 150, 70, and 5.5 K) show constant boost of 33% and 25% for (e) nFET and (f) pFET, respectively.**

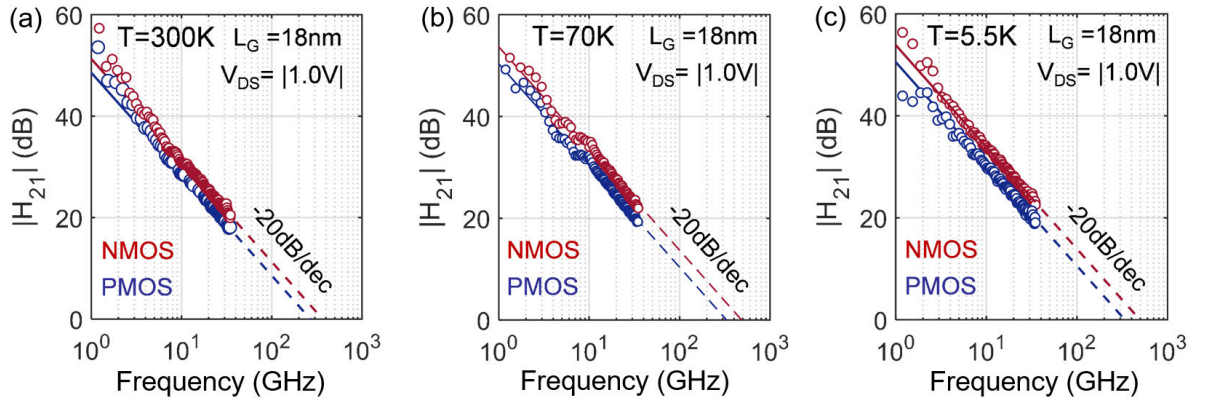

FIGURE 4. **Extraction of f_T from −20 dB/dec extrapolation of access/pad parasitic de-embedded short-circuit current gain ($|H_{21}|$) to unity, under peak-g_m gate bias and $|V_{DS}| = 1$ V for 18 nm L_G NMOS (red) and PMOS (blue) at (a) 300, (b) 70, and (c) 5.5 K.**

Fig. 7(a)] and PMOS [see Fig. 7(b)]. Extrapolated peak-f_{MAX} was found to improve by 30% for both NMOS (from 373 GHz at 300 K to 497 GHz at 5.5 K) and PMOS (from 288 GHz at 300 K to 372 GHz at 5.5 K), as shown in Fig. 7(c). Accuracy of the de-embedding method used in this work is validated by the excellent agreement of extrapolated f_T and f_{MAX} at 300 K with reported values for 22 nm FDSOI FETs (nFET/pFET f_T 350/244 GHz, nFET/pFET f_{MAX} 370/277 GHz) [18]. It should be noted that drain current densities (I_{DS}/W) corresponding to both extrapolated peak-f_T and peak-f_{MAX} are invariant of temperature.

C. SMALL-SIGNAL CIRCUIT MODEL FOR CRYOGENIC FDSOI

A small-signal equivalent circuit model was used to capture the cryogenic RF performance of 18 and 28 nm L_G FETs

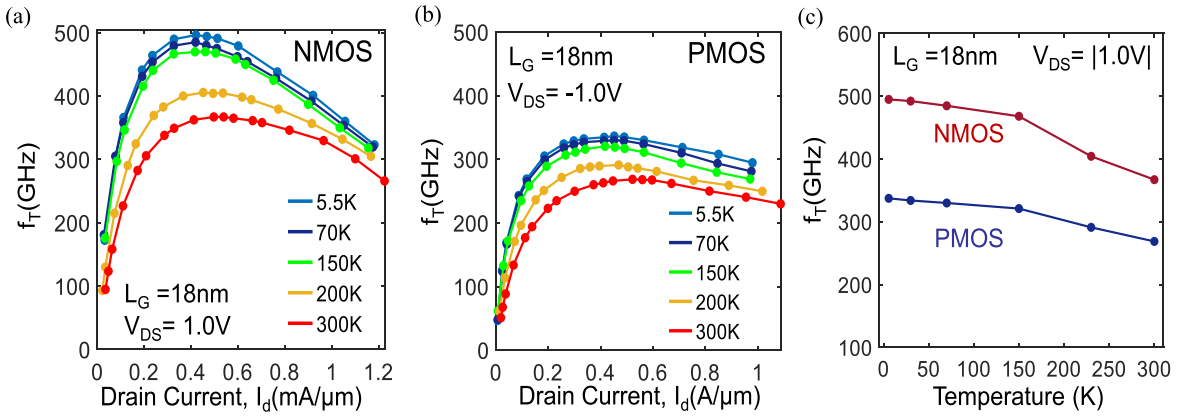

FIGURE 5. Drain-current (I_{DS}/W) dependence of extrapolated f_T over the temperature range 300 to 5.5 K for 18 nm L_G. (a) NMOS and (b) PMOS, under $|V_{DS}| = 1$ V. (c) Extrapolated peak-f_T as a function of temperature show boost of 35% (to 495 GHz) and 25% (to 337 GHz) at 5.5 K for NMOS and PMOS, respectively.

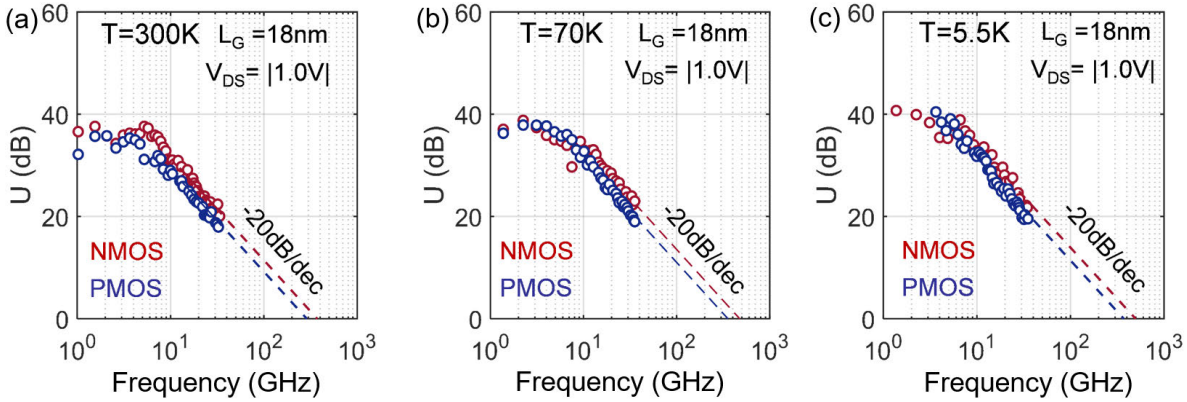

FIGURE 6. Extraction of f_{MAX} from −20 dB/dec extrapolation of access/pad parasitic de-embedded Unilateral power gain (|U|) to unity, under peak-g_m gate bias and $|V_{DS}| = 1$ V for 18 nm L_G NMOS (red) and PMOS (blue) at (a) 300, (b) 70, and (c) 5.5 K.

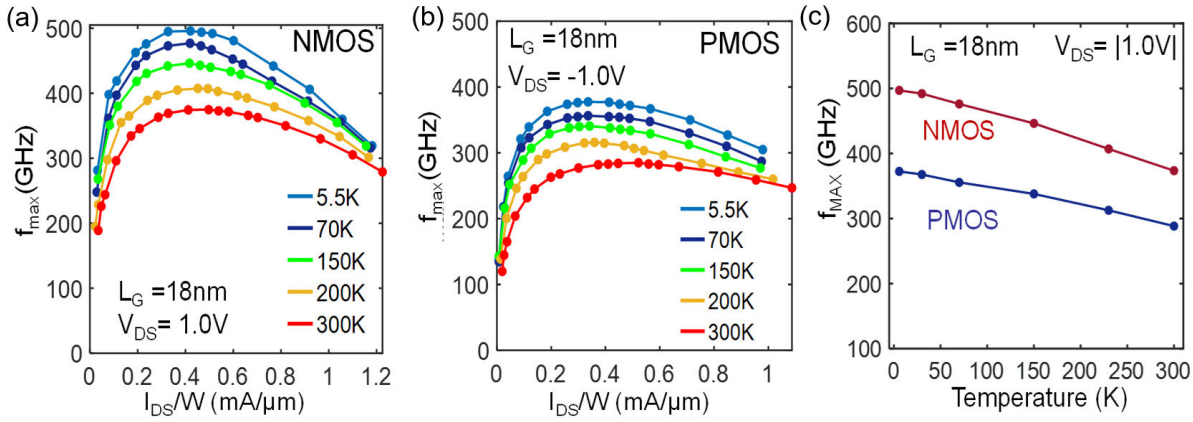

FIGURE 7. Drain-current (I_{DS}) bias dependence of extracted f_{MAX} over the temperature range 300–5.5 K for 18 nm L_G. (a) NMOS and (b) PMOS, under $|V_{DS}| = 1$ V. (c) Peak f_{MAX} as a function of temperature show f_{MAX} boost of 30% to 497 and 372 GHz at 5.5 K for NMOS and PMOS, respectively.

for a bias condition of $|V_{DS}| = 1$ V and a $|V_{GS}|$ corresponding to the peak-g_m. Fig. 8(a) summarizes the access parasitic capacitances embedded within the RF test structure, along with interconnect-line parasitic, extrinsic, and intrinsic FET parameters shown in Fig. 8(b). The reference plane for the available RF test structure is the M1 metal layer. The small-signal equivalent circuit model includes interconnect-line and access parasitic, along with extrinsic and intrinsic FET elements for accurately extracting RF FoMs of 22 nm cryogenic FDSOI technology, as shown in [see Fig. 8(c)]. Extrinsic FET circuit elements include external resistances (R_{de}, R_{se}, R_{ge}) and capacitances (C_{gse}, C_{gde}, C_{dse}) associated with individual FET terminals, whereas the intrinsic FET parameter set consists of intrinsic transconductance ($g_{m,int}$), intrinsic terminal capacitances (C_{gsi}, C_{gdi}, C_{sdi}), and output conductance (g_o). Measured and modeled

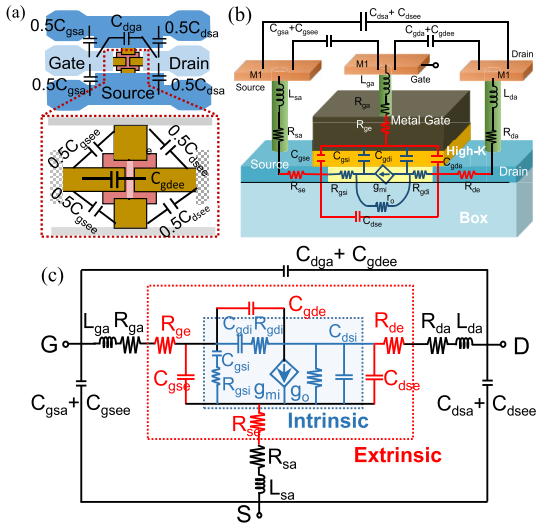

FIGURE 8. (a) Different access and pad parasitic in RF test structure. (b) Schematic and (c) small-signal equivalent circuit model of 22 nm FDSOI FET with illustration of access/ interconnect parasitic, extrinsic, and intrinsic FET.

S-parameters for 18 nm L_G NMOS and PMOS show excellent agreement across the entire temperature range, as highlighted in Fig. 9(a)–(f). The access capacitance and inductance elements were found to be temperature invariant, whereas interconnect-line resistance was reduced at low temperatures. However, due to infinitesimally low value (<3 Ω), these parameters were not found to have a significant effect on the measured S-parameters across temperatures.

Small-signal equivalent model parameters for 18 nm L_G n and p FDSOI at 300, 70, and 5.5 K are listed in Table 1. Fig. 10 summarizes the temperature and gate length dependence of small-signal equivalent model parameters. The intrinsic g_m improves by 39%/28% for NMOS/PMOS due to reduced phonon scattering at low temperature [19], as shown in Fig. 10(a). However, SR scattering slows the rate of improvement in $g_{m,\mathrm{int}}$ below 150 K, which is also consistent with the cryogenic measurement result. Source–drain series resistance (R_{se}, R_{de}) are found to be invariant of gate length and improves by 11%/12% for NMOS/PMOS at low temperature due to reduced sheet resistivity of source/drain extension [20], but saturates below 100 K [see Fig. 10(b)]. Simultaneous improvement in $g_{m,\mathrm{int}}$ and R_{se}, R_{de} contributes to the observed boost in f_T. $C_{\mathrm{gg},i}$ scales with gate length whereas $C_{\mathrm{gg},e}$ has no gate length dependence [see Fig. 10(c) and (d)]. Both the intrinsic and extrinsic gate capacitances ($C_{\mathrm{gg},i}$ and $C_{\mathrm{gg},e}$ respectively) remain almost invariant with temperature for NMOS and PMOS, whereas the gate-resistance (R_{ge}) decreases monotonically by 32%/24% for NMOS/PMOS [see Fig. 10(e)] due to reduced resistivity of gate metal contact (NiSi) and poly-Si at a cryogenic temperature [21]. The combined effect of improvement in f_T and R_{ge} explains the improvement in f_{MAX} at low temperature. Output conductance (g_o) however increases at low temperature [see Fig. 10(f)], due to slightly degraded short channel effect (SCE) likely from partial channel dopant

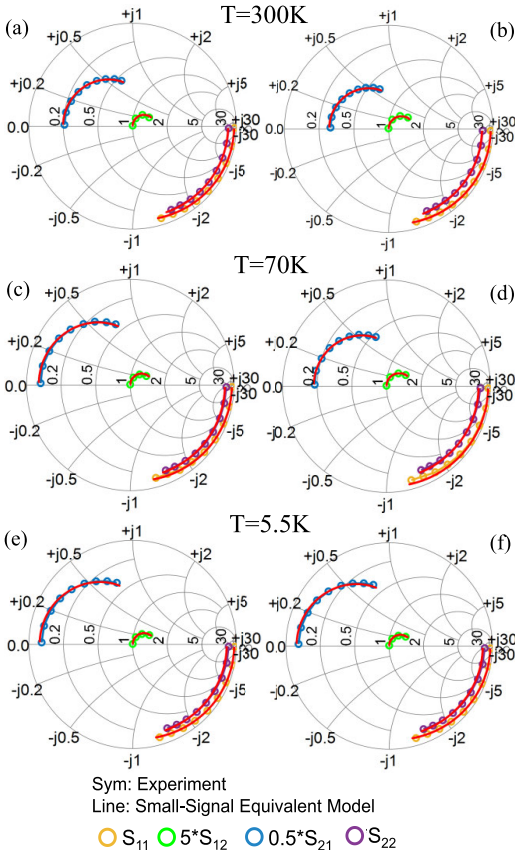

FIGURE 9. Modeled (solid line) S-parameters using small-signal equivalent circuit model show perfect agreement with measured S-parameters (symbol) from 0.5–35 GHz for 18 nm gate length *n*-FDSOI at (a) 300, (c) 70, and (e) 5.5 K and p-FDSOI at (b) 300, (d) 70, and (f) 5.5 K for V_{DS} = 1.0 V and V_{GS} at maximum g_m.

de-activation in the channel.

However, small-signal equivalent circuit model parameters for cryogenic-RF FDSOI were extracted with reference to the M1 (metal 1) plane. Hence, it should be noted that effective values of the model parameters and also extracted f_T/f_{MAX} may vary depending on the connection of the extrinsic transistor to different metal layers present in an actual circuit. Cryogenic characterization and circuit model implementation of different interconnect layers is hence required to allow the accurate design of cryogenic-RF CMOS. Also, intrinsic transconductance ($g_{m,i}$) in this work has been considered as a real number. However, a phase factor associated with $g_{m,i}$ can also be included for capturing the non-quasi-static response of the small-signal equivalent circuit model [22], in order to allow operation at higher frequencies (>100 GHz).

D. DELAY-TIME ANALYSIS OF CRYOGENIC-RF FDSOI

A delay-time analysis is performed to identify the contribution of different delay subcomponents on f_T improvement at 22 nm FDSOI FETs at cryogenic temperature [23]. The analytical expression of f_T can be obtained from the small-signal

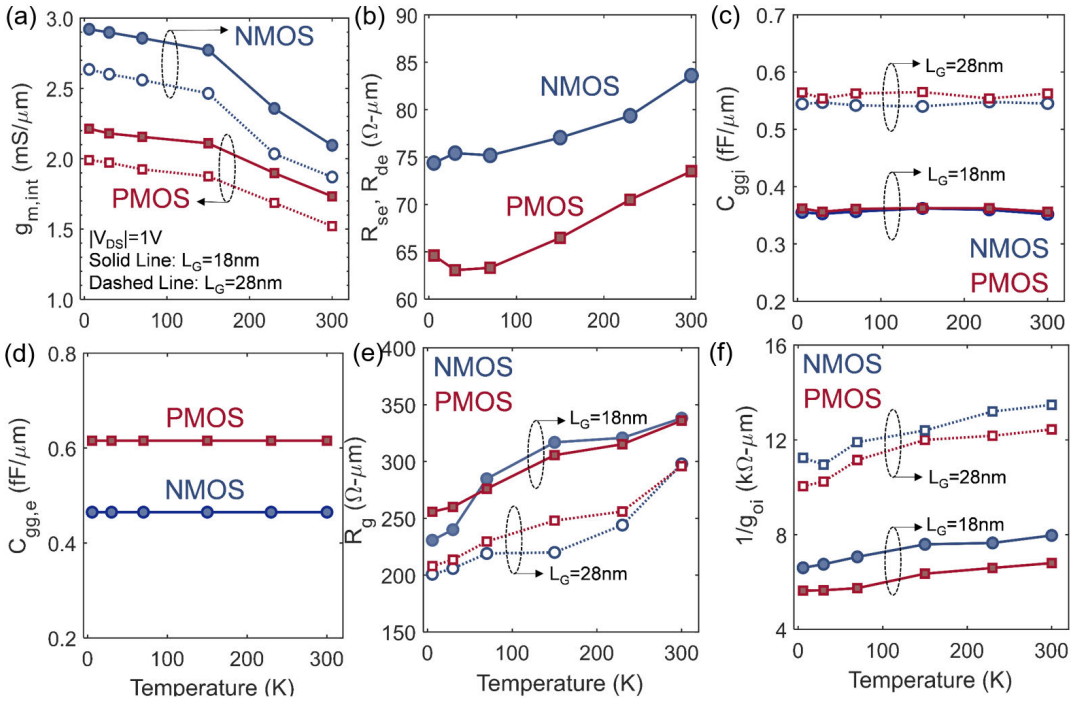

FIGURE 10. (a) Intrinsic g_m ($g_{m,\text{int}}$) improves at low temperature in NMOS and PMOS due to reduced phonon scattering. (b) Source/drain series resistance (R_{se}, R_{de}) improve by 15% at 5.5 K. (c) Intrinsic ($C_{\text{gg},i}$) and (d) extrinsic ($C_{\text{gg},e}$) component of gate-capacitance ($C_{\text{gg},T} = C_{\text{gg},i} + C_{\text{gg},e}$) remains invariant with temperature. (e) Reduced resistivity of gate metal contact (NiSi) and poly-Si cause gate resistance (R_{ge}) reduction at cryogenic temperature. (f) Channel conductance (g_o) increase by 25% at low temperature.

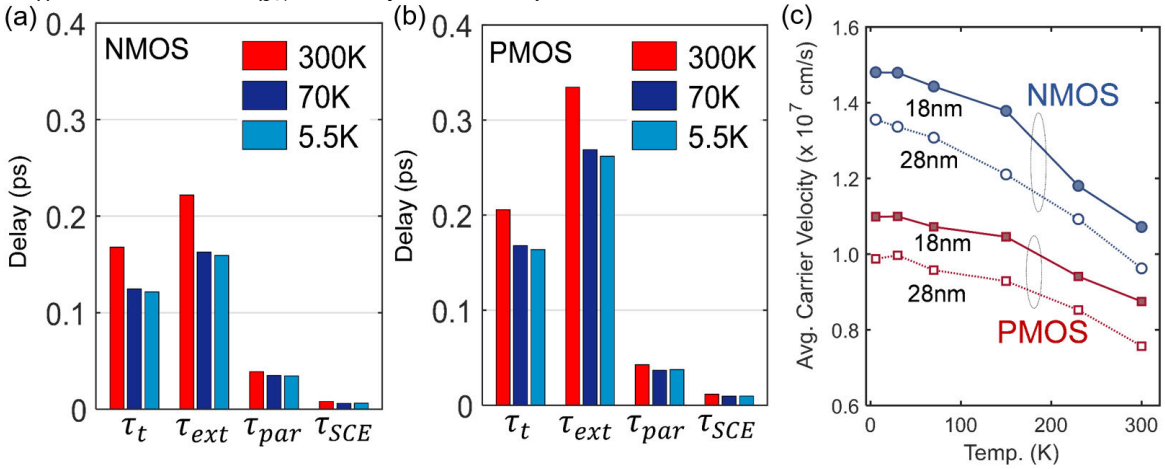

FIGURE 11. Delay-time analysis shows 38%/25% improvement in intrinsic transit time (τ_t) and 40%/27% improvement in external parasitic delay (τ_{ext}) at 5.5 K compared to 300 K for 18 nm L_G (a) NMOS and (b) PMOS, respectively. (c) Improved transit time can be attributed to enhanced average electron and hole velocity at cryogenic temperature in NMOS and PMOS, respectively.

equivalent circuit model as

$$2\pi f_T = \frac{g_{m,i}}{C_{\text{gg},T} + g_{m,i}R_{\text{sde}}\left[C_{\text{gdi}} + C_{\text{gde}} + \frac{g_o}{g_{m,i}}\left(C_{\text{gg},T}\right)\right]}. \tag{2}$$

The total delay ($\tau_{\text{Delay}} = 1/2\pi f_T$) can hence be partitioned into four components, such as intrinsic transit time (τ_t), extrinsic charging delay (τ_{ext}), parasitic delay (τ_{par}), and delay due to short-channel effect (τ_{SCE})

$$\tau_{\text{Delay}} = \tau_t + \tau_{\text{ext}} + \tau_{\text{par}} + +\tau_{\text{SCE}} \tag{3}$$

where, $\tau_t = (C_{\text{gg},i}/g_{m,i})$, $\tau_{\text{ext}} = (C_{\text{gg},e}/g_{m,i})$, $\tau_{\text{par}} = R_{\text{sd},e} \cdot C_{\text{gd},e}$, and $\tau_{\text{SCE}} = (R_{sd,e} \cdot (C_{\text{gg},Ts}) \cdot g_o/g_{m,i})$.

Transit time (τ_t) can be calculated as the ratio of channel length (L_{Ch}) and average velocity of carriers (v_{Avg}) in the channel. Hence, the observed improvement in transit time can be attributed to enhanced average carrier velocity at cryogenic temperature for both NMOS and PMOS [24]. Fig. 11(c) summarizes the enhancement in v_{Avg} due to faster electron and hole transport in n and p-MOSFETs (L_G 18 and 28 nm), respectively. Improvement in $g_{m,\text{int}}$ enables a reduction in τ_{ext} as $C_{\text{gg},e}$ remains invariant with temperature. τ_{par} also scales with temperature due to reduced R_{se}, R_{de}. Moreover, τ_{SCE} improves down to 70 K due to improved $g_{m,\text{int}}$ but slightly degrades at lower temperature as g_o also increases. Hence reducing the extrinsic device parasitic capacitance (low-k spacer), reducing source/drain series resistance, and

TABLE 1. Extracted Extrinsic and Intrinsic Parameters for RF Small-Signal Model.

		NMOS (L_G=18nm)			PMOS (L_G=18nm)		
Temp.		300K	70K	5.5K	300K	70K	5.5K
Extrinsic Parameters	R_{se}/R_{de} (Ω-μm)	83.59	75.17	74.36	73.51	63.31	64.61
	R_{ge} (Ω-μm)	338	285	231	336	276	256
	C_{gse} (fF/μm)	0.233	0.233	0.233	0.312	0.312	0.312
	C_{gde} (fF/μm)	0.164	0.164	0.164	0.27	0.27	0.27
	C_{dse} (fF/μm)	3.2×10^{-3}	3.2×10^{-3}	3.2×10^{-3}	6.2×10^{-3}	6.2×10^{-3}	6.2×10^{-3}
Intrinsic Parameters	g_{mi} (mS/μm)	2.1	2.86	2.92	1.73	2.16	2.21
	$1/g_{oi}$ (kΩ-μm)	7.96	7.05	6.60	6.80	5.73	5.63
	R_{gsi} (Ω-μm)	0.12	0.090	0.075	0.12	0.090	0.075
	R_{gdi} (Ω-μm)	0.80	0.69	0.38	0.80	0.69	0.38
	C_{gsi} (fF/μm)	0.352	0.355	0.356	0.356	0.361	0.361
	C_{gdi} (fF/μm)	1.2×10^{-4}	1.2×10^{-4}	1.2×10^{-4}	6.2×10^{-4}	6.2×10^{-4}	6.2×10^{-4}
	C_{dsi} (fF/μm)	1.2×10^{-4}	1.2×10^{-4}	1.2×10^{-4}	1.2×10^{-4}	1.2×10^{-4}	1.2×10^{-4}

TABLE 2. Performance Benchmarking of Advanced Node Cryogenic-CMOS Technology.

	28nm Bulk-Si [IEDM'19] [20]	**14nm FinFET [VLSI'20] [25]**	**28nm FDSOI [ESSDERC'17] [26]**	**28nm FDSOI [JEDS'20] [10]**	**22nm FDSOI [RFIC'19] [11]**	**22nm FDSOI [This work]**
L_G (nm)	30	15-23	28	25	20	18
V_{DD} (V)	0.8	0.75	0.9	1.0	0.8	1.0
n/p SS at 77K (mV/dec)	30/36	25/26	25/25	-	-	26/28
n/p $g_{m,\ Lin}$ @77K	+37%/+35 %	+55%/+49%	+66%/+67%	-	-	+60%/+71%
n/p $g_{m,\ Sat}$@77K	+19%/20%	+24%/+16%	+27%/+35%	33%/ -	+30%/+27%	+38%/+27%
n/p f_T (GHz)	-	-	-	400/- (at 4.2K)	380/240 (at 3.3K)	495/337 (at 5.5K)
n/p f_{Max} (GHz)	-	-	-	225/- (at 4.2K)	225/155 (at 3.3K)	497/372 (at 5.5K)

improving SCE through thinner body, scaled equivalent oxide thickness (EOT) are potential pathways to further improve the RF performance of 22 nm FDSOI technology at cryogenic temperature.

IV. CONCLUSION

In this work, we demonstrate record RF FoMs such as f_T of 495/337 GHz and f_{MAX} of 497/372 GHz for NMOS/PMOS at 5.5 K, on 22 nm FDSOI platform. This improvement is attributed to a 39%/28% boost in intrinsic g_m as well as 11%/12% lower source–drain external series resistance (R_{se}, R_{de}) and 32%/24% lower gate resistance (R_{ge}) for NMOS/PMOS at cryogenic temperature. Output conductance increased by 17% for both NMOS and PMOS at cryogenic temperature, with no significant effect on f_T. Furthermore, the back-biasing capability of 22 nm FDSOI technology can be utilized for V_{TH} tunability at cryogenic temperature. A small-signal equivalent circuit model was used to extract the temperature variation of intrinsic and extrinsic transistor parameters for 22 nm FDSOI technology down to deep-cryogenic temperature (5.5 K). This paves a pathway for design-space exploration of high gain-bandwidth mixed-signal circuits for cryogenic RF applications. Performance benchmarking of cryogenic CMOS technologies, as listed in Table 2, reveal that 22 nm cryogenic-RF FDSOI FETs showcased in this work provide superior f_T, f_{MAX} for both NMOS and PMOS, and hence are an excellent option for achieving superior analog performance with high transistor density at cryogenic temperature.

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[1] Registered trademark

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